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Davor Mance

Development of Electronic System for Sensing and Actuation of Test Mass of the Inertial Sensor LISA

Razvoj Elektroničkog Sustava za Očitavanje i Pokretanje Test Mase Inercijalnog Senzora LISA

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SAŽETAK i KLJUČNE RIJEČI

Razvoj Elektroničkog Sustava za Očitavanje i Pokretanje Test Mase Inercijalnog Senzora LISA

SAŽETAK: Detekcija gravitacijskih valova na frekvencijama nižim od 10 mHz zahtijeva referentni senzor inercijalnog sustava instaliranog u svemiru sa neouporedivom preostalom, sopstvenom akceleracijom i opto-elektronički sustav sposoban mjeriti izvannredno male devijacije prostora između dva referentna senzora udaljena nekoliko miliona kilometara. Test masa, korištena kao reflektirajuće ogledalo takvog gravitacijskog, opto-elektroničkog detektora, referentni je senzor a čelna elektronika inercijalnog senzora, elektronički sustav potreban za očitavanje pozicije test mase u svemirskom brodu i njeno pokretanje po svim stupnjevima slobode kretanja osim glavne mjerne osi za detekciju gravitacijskih valova.

Otuda se problem postignuća zanemarive akceleracije test mase prevodi u konstrukcijske elektroničke zahtjeve za ekstremno malom razinom šuma očitavanja njene pozicije, kontroliranim povratnim silama, i s tim u vezi krutošću, između kruga za očitanje i test mase, te izvanredno visokom stabilnošću signala za njeno pokretanje. Zbog prirode elektroničkog šuma i njegovog rasta pri niskim frekvencijama posebno je teško postići zahtijevane performanse ispod 1 mHz, te je to jedan od glavnih izazova u konstrukciji elektronike.

Stoga je rad na ovoj disertaciji postavljen s ciljem analiziranja i prevođenja glavnih zahtjeva svemirske misije u odgovarajuće elektroničke zahtjeve, definiranja osnovnih konstrukcijskih vodilja i uz njih vezanih tehnoloških izazova na polju kapacitivnog mjerenja i elektrostatičkog djelovanja, vrednovanja i verificiranja konstrukcijskih opcija izradom i testiranjem elektroničkih krugova te sakupljanjem postignutih saznanja i naučenih lekcija u cilju razvoja elektronike za konačnu upotrebu u svemiru i buduća istraživanja na tom polju. Osnovna teza disertacije mogućnost je postignuća izazovnih elektroničkih zahtjeva na frekvencijama ispod 10 mHz, posebno šuma kapacitivnog očitavanja ispod $1\,aF/\sqrt{Hz}$ i stabilnosti amplitude pokretanja test mase bolje od $2\,ppm/\sqrt{Hz}$. Minimalni ciljevi disertacije postavljeni su prema zahtjevima misije LISA Pathfinder, predhodnici LISA misije i performansama vezanih za 1 mHz, dok su ciljne performanse LISA misije pri frekvenciji od 0,1 mHz analizirane u toku rada i dopunjene sugestijama za njihovo ostvarenje u toku budućeg razvoja.

U razradi konstrukcije kruga očitavanja razvijeno je nekoliko analitičkih modela rezonancijskog mosta na bazi diferencijalnog transformatora i kruga pred-pojačala, od jednostavnih do kompletnih, u cilju analize šuma, asimetrije mosta i analize temperaturne osjetljivosti parametara kruga. Modeli su provjereni simulacijama, korištenjem standardnih SPICE, npr. MicroCap simulatora za elektroničke krugove. Posebna pažnja usmjerena je u razvoj diferencijalnog transformatora očitavanja kao kritičnog čindbenika performansi. Slično tome, u domeni pokretanja test mase razmatrani su krugovi naponskog pojačala, dvije opcije generatora valnih signala i digitalnog regulatora i njihove su performanse valorizirane.

Izrađena su dva prototipa elektronike s početnim i poboljšanim performansama potvrđujući da je moguće postići pretpostavljene zahtjeve pri frekvenciji od 1 mHz, ali da je potreban dodatni rad na području stabilnosti naponske reference kako bi se postigao stupanj performansi kod krugova očitavanja i pokretanja pri 0,1 mHz.

KLJUČNE RIJEČI: LISA, LTP, IS-FEE, kapacitivno očitavanje, elektrostatičko pokretanje, šum niskih frekvencija, gravitacijski senzor

ABSTRACT and KEYWORDS

Development of Electronic System for Sensing and Actuation of Test Mass of the Inertial Sensor LISA

ABSTRACT: The detection of gravitational waves at frequencies below 10 mHz requires a reference sensor of the spaceborne inertial system with unprecedented residual acceleration and an optoelectronic system able to detect exceptionally small deviations of space between two reference sensors several million kilometers apart. The test mass, used as a reflecting mirror of such a gravitational optoelectronic detector, is the reference sensor, and the inertial sensor front-end electronics are the electronic system necessary to sense the position of the test mass in the spacecraft and to actuate it in all degrees of freedom, except the main measurement axis used for gravitational wave detection.

Hence, the problem of achieving a negligible test mass acceleration translates into the electronics design requirements with an extremely low sensing noise, controlled back-action forces and related stiffness between the sensing circuit and the test mass and an exceptionally high stability of actuation signals. Due to the nature of the rising electronics noise at low frequency, it is particularly difficult to achieve the requirements below 1 mHz, which is the major challenge in the electronics design.

Therefore, a work covered by this dissertation has been launched aiming to analyze and convert the top-level mission requirements into electronics requirements, define the main design drivers and related technological challenges in the field of capacitance measurement and electrostatic actuation, evaluate the design options, verify selected designs by building and testing the hardware and collect the acquired knowhow and lessons learned for flight hardware development and future research in this field. The dissertation goal is set to show how it is possible to achieve the challenging electronics requirements at frequencies below 10 mHz, in particular a capacitive sensing noise performance below $1\,aF/\sqrt{Hz}$ and an actuation amplitude stability better than $2\,ppm/\sqrt{Hz}$. During the work, the minimum performance goal was set to achieve the LISA Pathfinder mission requirements at 1 mHz, but the ultimate goal of LISA mission at 0,1 mHz has been analyzed throughout the work leading to a set of design suggestions for future developments.

In the elaboration of the sensing circuit design, several analytical models of the resonant sensing transformer bridge and the preamplifier circuits, from simple to complete, were developed to analyze the noise sources, bridge asymmetries and temperature sensitivities of the circuit parameters. The models were verified by the circuit simulation using standard SPICE, e.g., MicroCap simulators. Special attention has been given to the development of the differential sensing transformer, being the critical performance driver. Similarly, in the analysis of the actuation circuits, the drive voltage amplifier, two waveform generators and controller options were considered and their performance analyzed.

Two breadboards were built with initial and improved performance, showing that it is possible to achieve postulated performance limits at 1 mHz and that additional work is needed on voltage reference stability to achieve the required performance in both sensing and actuation circuits at 0,1 mHz.

KEYWORDS: LISA, LTP, IS-FEE, capacitive sensing, electrostatic actuation, low-frequency noise, gravitational sensor

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First of all, I would like to thank all those who contributed to this dissertation in one way or another. In particular, I cannot omit to express my gratitude to all my colleagues who were involved in the work described in it. The writing of the dissertation was an extraordinary experience for me, both professionally and personally.

Above all, I need to thank Domenico Giardini and Peter Zweifel, who offered me the great opportunity to join the Institute and to work on space projects within the ETH, Zurich. Domenico's ability to coordinate our group activity made our work fruitful and enjoyable, and helped us overcome many challenges. I remember taking part in numerous project meetings with Peter and discussing the LISA Pathfinder electronics development for hours at a time with him. Parts of this long story are embodied in the dissertation.

I spent a lot of time working with Franz Weber, who did most of the detail work by building the test jigs, numerous transformer coils and printed circuits boards of the first breadboard with care, patience and precision. I certainly appreciate his devotion to the task and his pleasant attitude, which helped us get through the long experimentation period. Similarly, my thanks go to Daniel Strässler for building the second breadboard.

I would also like to thank my colleague Jan ten Pierick for his contribution to the digital controller design and my colleague Li Gan for testing the hardware, collecting data and providing initial support in the writing of the dissertation.

Special thanks go to Stefano Vitale and Bill Weber from the University of Trento. I greatly benefited from their competence and devotion, which contributed to the success of this fascinating space project. I remember my many email exchanges with Bill and the sketches he drew during our meetings that helped me understand the physics behind the design of the electronics. He transferred most of the know-how relating to this project to me.

This work would not have ended up in the form of a dissertation if it had not been initiated by the Department of Electronics of the Faculty of Engineering at the University of Split. My gratitude goes to my mentor, Jadranka Marasović, and my co-mentor, Nikola Godinović, who helped me complete the work.

And finally, the most loving thanks are dedicated to Nira for the patience, encouragement and understanding she showed while I was going through this process, and to Jas for putting the finishing touch on the dissertation.

PREFACE

The main concern of this dissertation is the development of electronics for attitude sensing and controlling a reference body in space that is used to detect gravitational waves. For this purpose, electronics with very low noise will be used, particularly at low frequency. In the dissertation, the electronics design for the capacitive sensing and the electrostatic actuation of the reference body was analyzed, electronics performance estimated by simulation and finally verified using breadboard electronics.

The dissertation comes as a result of the research work carried out at the Institute of Geophysics – Swiss Federal Institute of Technology in Zurich (ETHZ) and the Institute for Theoretical Physics – University of Zurich (UNIZ).

The work was initiated by the development of an European Space Agency (ESA) space mission, named LISA Pathfinder (LPF), which ETHZ and UNIZ joined in 2003. The LISA Technology Package (LTP) is the scientific instrument on board the LPF in which the reference body is controlled by the Inertial Sensor Front-End Electronics (IS-FEE). Developing the IS-FEE was the task of the Institute of Geophysics, while the astrophysical aspects of the mission were managed by the Institute for Theoretical Physics. Financial support was provided by the Swiss funding for space projects to cover the Institute's research and the industrial costs of manufacturing flight hardware.

The preparatory work, carried out during the first two years, included the definition of electronics requirements, selection of industrial partners and initial research at ETHZ laboratories. Also, the first electronics breadboards were built and performance was verified during this time. The dissertation encompasses mostly this initial research and design work. In later phases, the development of flight hardware shifted to the industry, with continuous ETHZ supervision and assistance with technical aspects. The flight hardware development path included manufacturing an Engineering Model (EM) and a Proto Flight Model (PFM). The industrial phase was completed with the delivery of the PFM at the end of 2009. ETHZ continued to assist with the integration and testing of the hardware at upper levels of integration and provided detailed electronics modeling support to ESA. ETHZ cooperated with other institutes throughout the development of the mission, in particular with the Department of Physics at the University of Trento (UTN). Prof. Stefano Vitale from UTN, the Principal Investigator (PI) of the mission, and his team provided crucial help and initial guidance for IS-FEE development.

The dissertation is divided into six main chapters: introduction, development of sensing electronics, development of actuation electronics, breadboard electronics design with performance evaluation, conclusions and future work. A short description of the chapters is provided below in order to enable the reader to follow the presented material more easily.

In Chapter 1 an introductory context of electronics development is provided, namely, their role in the detection of gravitational waves and a short description of the LISA and LPF missions. Furthermore, the main tasks of electronics are described and development guidelines set. Previous work in related fields is noted in an attempt to establish a correlation with the required additional work, that work being the major motivation for this research. Upon recognition of the complexity of the work, the main goals and objectives are defined.

The sequence of the dissertation is then explained along with the necessity of the required research phases. The main contribution of the dissertation is stated at the end of the chapter.

The design of sensing and actuation electronics is provided in Chapter 2 and Chapter 3, respectively. Work begins with an analysis of the main functional and performance requirements, which constrain electronics architecture and possible solutions. A detailed design of each block is then made and supported by theoretical analysis and the modeling of foreseen circuits. Lastly, performance is analyzed using SPICE-type simulations. Where several design solutions were possible, each was analyzed and evaluated so as to achieve an optimal tradeoff with respect to the constraints of the project, such as power and performance.

Chapter 4 deals with the verification of the developed electronics. This is done by manufacturing crucial circuits, the breadboard electronics, by testing electronics and by analyzing their performance. The major design goal in the initial phase was the performance rather than the reduction of power or strict use of space-qualified parts. Therefore, the breadboard was made with commercial parts, which are based on new technology compared with the relatively old parts with space heritage. Space-qualified parts would also largely affect the costs and the development time.

Conclusions and readiness to proceed with flight hardware manufacturing are given in Chapter 5. Several directions for future work on the LISA mission, whose requirements will be ten times as challenging to meet, are given in Chapter 6.

At the end, the dissertation is equipped with appendices, notation and references to which links are provided throughout the text. In addition, the author's resume and an abstract of the dissertation with keywords are provided in the English and Croatian languages, according to the guidelines set by the Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture – University of Split (FESB).

The material presented in the dissertation relates to several publications and technical notes either authored or co-authored by me during a project I worked on. They are either available externally or archived in the ESA project documentation repository.

Below, only the publications and technical notes that were published during this research work and are closely linked to the dissertation are provided in chronological order:

Publications:

The LTP experiment on the LISA Pathfinder mission, 2005
LISA Pathfinder: the experiment and the route to LISA, 2009
Data analysis for the LISA Technology Package, 2009
The first mock data challenge for LISA Pathfinder, 2009
From laboratory experiments to LISA Pathfinder: achieving LISA geodesic motion, 2010
Actuation to sensing crosstalk investigation in the inertial sensor front-end electronics of the laser interferometer space antenna pathfinder satellite, 2011
LTP IS FEE sensing channel: front-end modeling and symmetry adjustment method, 2011

Technical notes:

S2-ETH-RS-3001_IS-FEE requirements document, 2006 (first issue in 2003)
S2-ETH-TN-3002_Actuation to sensing cross-coupling analysis, 2005
S2-ETH-TN-3003_Conventional and bifilar transformer comparison, 2005
S2-ETH-TN-3004_Sine actuation waveforms, 2005
S2-ETH-TN-3005_Update of actuation to sensing cross-coupling analysis, 2005
S2-ETH-TN-3006_Orthogonality of actuation waveforms, 2005

S2-ETH-TN-3007_Update of sine actuation waveforms, 2005
S2-ETH-TN-3008_Pulsed versus sine actuation, 2005
S2-ETH-TN-3009_Sensing front-end redesign, 2006
S2-ETH-TN-3010_Actuation passive AC - DC splitter, 2006
S2-ETH-TN-3011_Sensing noise dependency on capacitance variation, 2006
S2-ETH-TN-3012_Actuation loop controller, 2006
S2-ETH-TN-3013_Sensing bits and noise, 2006
S2-ETH-TN-3014_Sensing noise limits and measurements, 2006
S2-ETH-TN-3015_Discrete JFET sensing preamplifier, 2006
S2-ETH-TN-3016_HEV sensing transformer parameters measured by ETHZ, 2006
S2-ETH-TN-3017_FEE SAU sensitivity to sensing cable movement, 2006
S2-ETH-TN-3018_Sensing bridge tuning methods, 2006
S2-ETH-TN-3019_OP148 instability, 2006
S2-ETH-TN-3020_Sensing noise of ETHZ breadboard, 2006
S2-ETH-TN-3021_Sensing noise improvement of ETHZ breadboard, 2006
S2-ETH-TN-3022_Actuation to sensing cross-talk of ETHZ breadboard, 2007
S2-ETH-TN-3023_IS-FEE subsystem demodulator tuning and offset characterization, 2007
S2-ETH-TN-3024_IS-FEE ELM light grounding, 2007
S2-ETH-TN-3025_IS-FEE bipolar sensing gain symmetry, 2007
S2-ETH-TN-3026_IS-FEE sensing offset sensitivity to bridge parameters, 2007
S2-ETH-TN-3027_I1.0_IS-FEE actuation stability characterization, 2008
S2-ETH-TN-3028_I1.0_IS-FEE actuation model and quantization effects, 2009
S2-ETH-TN-3029_IS-FEE PFM actuation stability characterization, 2010
S2-ETH-TN-3030_IS-FEE PFM actuation stability characterization re-test, 2010

The primary motivation for this dissertation was to summarize in one place all my research and design work on LTP IS-FEE electronics development and thus set a baseline for future development of the LISA Gravitational Reference Sensor (GRS) electronics.

Zurich, November 2011

Davor Mance

CONTENTS

LIST OF TABLES

LIST OF FIGURES

NOTATION

ABBREVIATIONS

AC	alternating current
A/D	analog to digital
ADC	analog to digital converter
ASD	amplitude spectral density
ASTRE	Accéléromètre Spatial TRiaxial Electrostatique
BB	breadboard
BNC	bayonet Niell-Concelman (coaxial connector)
BW	bandwidth
CAESAR	Capacitive and Electrostatic Sensitive Accelerometer Reference
COTS	commercial-of-the-shelf
DAC	digital to analog converter
DC	direct current
DEMC	demodulator control
DFACS	Drag-Free Attitude Control System
DMM	digital multimeter
DNL	differential non-linearity
DOF	degree of freedom
DRS	Disturbance Reduction System
DSB-AM	double-sideband amplitude modulation
DUTY	duty factor
DVA	drive voltage amplifier
EEPROM	electrically erasable programmable read-only memory
EH	electrode to housing
EL	electrode
ELM	electrical model
EM	engineering model
EMI	electromagnetic interference
ENOB	effective number of bits
ESA	European Space Agency
ET	electrode to TM
ETHZ	Eidgenössiche Technische Hochschule, Swiss Federal Institute of Technology, Zürich
FEE	Front-End Electronics
FESB	Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture, Fakultet Elektrotehnike, Strojarstva i Brodogradnje
FET	field-effect transistor
FPGA	field programmable gate array
FSR	full-scale range
GBW	gain bandwidth
GEO	geosynchronous Earth orbit
GRADIO	gradiometer
GRS	Gravitational Reference Sensor
HES-SO	Haute Ecole Spécialisée de Suisse Occidentale, University of Applied Sciences of Western Switzerland
HEV (HEVs)	Haute Ecole Valaisanne (previous name of HES-SO)
HR	high resolution
INL	integral non-linearity
IS	inertial sensor
IS-FEE	Inertial Sensor Front-End Electronics
JFET	junction field effect transistor
LCGT	Large Cryogenic Gravitational Telescope
LF	low frequency
LIGO	Laser Interferometer Gravitational-wave Observatory
LISA	Laser Interferometer Space Antenna
LPF	LISA Pathfinder

LSB	least significant bit
LTP	LISA Technology Package
LUT	look-up table
MBW	measurement bandwidth
MIL	military
NASA	National Aeronautics and Space Administration
NG	noise gain
NPO	negative-positive zero (ceramic dielectric with the lowest capacitance to temperature dependence)
ONERA	Office National d'Etudes et de Recherches Aérospatiales
PC	personal computer
PCB	printed circuit board
PCU	power conditioning unit
PFM	proto flight model
PI	principle investigator
PID	proportional, integral and derivative
ppm	parts per million
PSD	power spectral density
PSR	pulsar
PTFE	Polytetrafluoroethylene (Teflon)
PWM	pulse width modulation
RMS	root mean square
RS	requirements specification
SAU	sensing and actuation unit
S/C	spacecraft
SINAD	signal to noise and distortion
SMD	surface mount device
S/N	signal to noise
SNR	signal to noise ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
SSU	sensor switching unit
TAMA	name of a Tokyo district around the National Astronomical Observatory of Japan
TDS	transformer design solution
THD+N	total harmonic distortion and noise
TIA	trans-impedance amplifier
TM	test mass
TN	technical note
TTL	transistor-transistor logic
ULE	ultra-low expansion
UNIZ	University of Zürich
USA	United States of America
UTN	University of Trento
VIRGO	Variability of Irradiance and Gravity Oscillations
VM	test mass voltage
WR	wide range

VARIABLES

A	electrode area; amplitude
$A, A(s)$	op-amp open loop gain transfer function
A_L	inductance factor
A_{OL}	op-amp DC open loop gain
a	acceleration
a_0	maximum actuation acceleration authority
a_n	TM acceleration noise
a_{x_max}	maximum acceleration in *x*-axis
a_{z_max}	maximum acceleration in *z*-axis
b	tuning coefficient
b_w	winding window breath
C_o	electrode capacitance for centered TM
$C_{1,2,3,4}$	capacitance of four sensing electrodes
C_{2x}	nominal capacitance of two electrodes in *x*-axis
C_{2z}	nominal capacitance of two electrodes in *z*-axis
$C_A, C_a, C_{a1,2}$	sensing bridge actuation filter capacitors
C_{BR0}	equivalent sensing bridge input capacitance due to the sensing offset
C_{BRS}	sensing bridge input capacitance (pure sensing signal without offset)
C_D	decoupling capacitor
C_d	distributed capacitance

C_{DIE}	capacitance of JFET die material
C_{el}	sensing electrode capacitance
C_{eq}	equivalent resonance tuning capacitance
C'_{eq}	C_{eq} including TIA input capacitance
C_{FB}	feedback capacitor
C_H	TM stray capacitance to ground (housing)
C_{IN}	op-amp input capacitance; main amplifier decoupling capacitor
C_{INC}	op-amp input common-mode capacitance
C_{IND}	op-amp input differential capacitance
C_{inj}	capacitance between TM and injection electrodes
$C_{ISS}(C_{GS})$	JFET common source (gate-source) input capacitance
C_j	TM to *j*-sensor surface capacitance
$C_p, C_{p1,2}$	sensing bridge parallel (tuning) capacitances
C'_p	C_p including TIA input capacitance
C_R	resonance tuning capacitance (same as C_p)
$C_{RSS}(C_{GD})$	JFET common source reverse transfer (gate-drain) capacitance
C_{tot}	total capacitance between TM and sensor surfaces
ΔC	differential sensing capacitance
$\partial C/\partial x$	capacitance gradient in *x*-axis
$\partial C_{EH}/\partial x$	electrode to housing (EH) capacitance gradient in *x*-axis
$\partial C_{ET}/\partial x$	electrode to TM (ET) capacitance gradient in *x*-axis
$\partial \Delta C/\partial x$	differential capacitance gradient in *x*-axis
$D(s)$	denominator complex function
d	nominal sensing gap; wire diameter
$\hat{d}(X)$	smoothing function
d_x	*x*-axis electrode gap
d_z	*z*-axis electrode gap
$DUTY$	duty cycle ratio
E	electrostatic energy
e	base of the natural logarithm
e_{BR_TH}	sensing output voltage noise due to the bridge thermal noise
e_{i-AMP}	equivalent voltage noise due to TIA current noise
e_N	equivalent input noise voltage
$e_{q\_ADC\_HR}$	ADC quantization noise in HR mode
$e_{q\_ADC\_WR}$	ADC quantization noise in WR mode
$e_{RMS-i_{AMP}}$	RMS voltage noise of op-amp current noise source
e_{RMS-TH}	RMS voltage noise of thermal noise source
$e_{RMS-u_{AMP}}$	RMS voltage noise of op-amp voltage noise source
e_{TH-ZBR}	thermal noise of the real part of sensing bridge impedance
e_{TH-ZFB}	thermal noise of the real part of the TIA feedback impedance
$e_{TIA-RMS}$	total TIA output RMS noise
e_{u-AMP}	TIA voltage noise
$F_{S/C}$	external spacecraft disturbing forces
F_{ba_x}	readout back-action force in *x*-axis
F_{max}	maximum actuation force
F_x	electrostatic force in *x*-axis
F_{x_max}	maximum force in *x*-axis
f	frequency
f_0	resonant frequency
f_c	carrier frequency
f_{CHOP}	chopping frequency
f_N	Nyquist frequency
f_{SR}	self-resonant frequency

f_{str}	stray force
$f(t)$	Fourier series function
$\partial F/\partial x$	force gradient causing deformation (displacement)
G	gain
$\hat{G}$	winding geometry parameter
G_0	sine waveform amplitude
$G_{HG,LG}$	main amplifier high, low gain
G_{TIA}	TIA gain; TIA transfer function
G_{TIA_id}	ideal TIA transfer function
G_{TIA_S}	simplified TIA transfer function
g_q	approximated sine waveform level of q[th] sample
H	magnetic field strength
h	gravitational wave amplitude (relative strain); number of higher harmonics in injection waveform; winding layer-to-layer separation
$H_{1,2}(\mathrm{s})$	actuation transfer functions of channel 1, 2
I	current; moment of inertia
$I_{1,2}$	electrode sensing currents in two arms of a bridge; currents through TIA input capacitances
I_{DSS}	JFET saturation drain current
I_{GSS}	JFET gate reverse (leakage) current
$I_{p1,2}$	transformer winding currents in a bridge
I_S	transformer secondary winding current
i	index (of a harmonic)
i_{AMP}	op-amp current noise
$i_{AMP+,-}$	op-amp current noise sources in non-inverting and inverting inputs
i_{DIE}	JFET noise due to the die material dielectric losses
$i_{FET+,-}$	JFET current noise sources
i_N	JFET current noise due to u_{FET}
i_{SL}	JFET gate leakage current shot noise
$\Im[Z_{BR}(\omega)]$	imaginary part of the complex bridge impedance
j	imaginary operator
$K, K_{1,2}$	primary to secondary transformer coupling coefficients
k, k_p	spring-like parasitic stiffness (coefficient)
$k_{1,2}$	transformer coupling-inductance coefficients; fitting coefficients
k_B	Boltzmann constant
L	distance; inductance
$L_{1,2}$	inductance of two primary windings of the bridge
L_{app}	apparent inductance
L_R	real inductance (with losses)
L_S	inductance of the secondary winding of the bridge; series inductance
LSB	least significant bit
LSB_{ADC}	ADC LSB size
LSB_{eff}	effective LSB size
LSB_{OUT}	output (processed) LSB size
ΔL	inductance asymmetry of transformer primary windings
$\Delta L/L$	relative inductance imbalance of the bridge
$(\Delta L/L)_{dc}$	relative DC inductance imbalance
δL	distance change
l	length of a winding
l_e	effective magnetic path length of the core
$\sum \frac{l}{A}$	magnetic form factor
M	spacecraft mass, mutual inductance
m	TM mass; number of approximation levels of sine waveform
$M_{i,j}$	mutual inductance between two transformer windings

$M_{1S,2S}$	transformer mutual inductance between primary 1, 2 and secondary winding
$m_{P,S}$	number of layers in the primary and secondary windings
N	number of turns in a winding; number of bits
N_0	noise amplitude
N_{in}	noise power at the demodulator input
N_{out}	noise power at the demodulator output
n	tuning coefficient
$n(t)$	noise before demodulation
$n_{1,2}$	number of turns of two transformer primary windings
$n_c(t)$	cosine (in-phase) component of the noise
$n_{LP}(t)$	low-pass filtered noise
n_S	number of turns of the transformer secondary winding
$n_s(t)$	sine (in-quadrature) component of the noise
NG	TIA noise gain
Q	quality factor
Q_{app}, Q_e	apparent, effective quality factor
q_0	number of electron charges accumulated on TM
q_e	electron charge
R	resistance; averaging ratio
$R_{a1,a2}$	actuation low-pass filter resistors of channel 1, 2
R_{app}	apparent resistance
R_{BR}	sensing bridge resistance (at resonance)
R_d	series resistance due to coil self-resonance and the distributed capacitance losses
$R_{d1,2}$	first and second components of R_d
R_{dc}	wire DC resistance
R'_{dc}	wire DC resistance per unit length
R_{ec}	equivalent resistance due to eddy current losses
R'_{ec}	equivalent resistance per unit length due to eddy current losses
R_{FB}	TIA feedback resistor
R_{IN}	main amplifier input resistor
R_L	resistive part of inductor
R_S	series resistance
R_{TOT}	total wire resistance
R_φ	φ-torque lever arm
r_{DS}	JFET drain-source resistance
$\Re[Z_{BR}(\omega)]$	real part of the complex bridge impedance
$\Re[Z_{FB}(\omega)]$	real part of the complex TIA feedback impedance
s	Laplace parameter; transformer core air gap
$S_a^{1/2}$	TM stray acceleration noise
$S_{a_{ACT}}^{1/2}$	TM acceleration noise due to FEE actuation noise
$S_{a\_act\_AC}^{1/2}$	TM acceleration noise due to actuation noise at actuation frequency, i.e. AC
$S_{a_x\_act\_AC}^{1/2}$	$S_{a\_act\_AC}^{1/2}$ in *x*-axis
$S_{a\_act\_amp}^{1/2}$	TM acceleration noise due to actuation amplitude stability
$S_{a\_act\_DC}^{1/2}$	TM acceleration noise due to actuation noise at low frequency, i.e. DC
$S_{a_{ba}}^{1/2}$	TM back-action acceleration noise
$S_c^{1/2}, S_{\Delta C}^{1/2}$	sensing capacitance noise
$S_{\Delta C-BR-th}^{1/2}$	capacitance thermal noise of the sensing bridge
$S_{DAC}^{1/2}$	total DAC relative output stability (noise)
$S_{DAC_B}^{1/2}$	DAC buffer relative output stability (noise)
$S_{DAC_R}^{1/2}$	DAC reference relative output stability (noise)
$S_{F_{ba}}^{1/2}$	TM back-action force noise

$S_h^{1/2}$	gravitational strain sensitivity
$S_{in}(\omega_0)$	input noise PSD at the carrier frequency
$S_{\Delta L/L}^{1/2}$	relative inductance imbalance fluctuation
$S_n(f)$	noise PSD
$S_{n_{LP}}(\omega_{LP})$	output noise PSD in the low-pass filter bandwidth
$S_{n_c}(\omega_0)$	cosine (in-phase) component of the noise PSD
$S_{n_s}(\omega_0)$	sine (in-quadrature) component of the noise PSD
$S_{out}(\omega_{LF})$	demodulated (filtered) output noise PSD
$S_T^{1/2}$	thermal fluctuation (noise)
$S_U^{1/2}$	quantization noise (voltage)
$S_u^{1/2}$	TIA output voltage noise
$S_{u\_AC}^{1/2}$	actuation AC voltage noise (at actuation frequency)
$S_{u-BR-th}^{1/2}$	voltage thermal noise of the sensing bridge
$S_{u\_DC}^{1/2}$	actuation DC voltage noise (in low-frequency measurement bandwidth)
$S_{\Delta U/U}^{1/2}$	actuation amplitude relative voltage stability (noise)
$S_{\partial U/U_M}^{1/2}$	TM injection relative voltage stability (noise)
$S_{\partial U/U_R}^{1/2}$	TM relative voltage reference amplitude stability (noise)
$S_x^{1/2}$	position (displacement) noise in *x*-axis
$S_{x-comb}^{1/2}$	position (displacement) noise of combined output
$S_{x,\Delta L}^{1/2}$	position noise due to inductance imbalance fluctuation
$S_{x_n}^{1/2}$	sensor position noise in *x*-axis
T	absolute temperature
$T_{1,2,3,4}$	time constants of $NG(s)$
$T_{ON,OFF}$	ON, OFF switching times
T_φ	electrostatic torque around *z*-axis
T_{φ_max}	maximum torque around *z*-axis
ΔT	temperature variation
TDS	transformer design solution
$tan\,\delta$	loss factor
$tan\,\delta_{Cd}$	dielectric losses in the wire insulation
$tan\,\delta/\mu_i$	relative loss factor
$U_{1,2}$	electrode voltages; TIA inverting input voltages
$U_{10,20}$	low-pass filtered actuation voltages from channel 1, 2
$U_{1x,2x}$	TM actuation voltages in *x*-axis (front and rear face)
$U_{1y,2y}$	TM actuation voltages in *y*-axis
$U_{1z,2z}$	TM actuation voltages in *z*-axis
$U_{1\eta,2\eta}$	TM actuation voltages around *y*-axis (left and right corner)
$U_{1\theta,2\theta}$	TM actuation voltages around *x*-axis
$U_{1\varphi,2\varphi}$	TM actuation voltages around *z*-axis
$U_{a1,a2}$	actuation voltages from channel 1, 2
U_{BR}	sensing bridge output voltage
U_{BR0}	sensing bridge output voltage (offset component)
U_{BRS}	sensing bridge output voltage (signal component)
U_Δ	voltage drop between TM and sensor surfaces
$U_{GS(off)}$	JFET gate-source cut-off voltage
U_{INJ}	injection voltage amplitude
U_j	*j*-electrode potential or actuation voltage
U_M	injected voltage on TM
U_{max}	maximum actuation voltage
U_O	TIA (differential) output voltage
$U_{o1,o2}$	output voltages of each TIA

U_{O_S}	simplified TIA output voltage
U_R	voltage reference amplitude
U_S	transformer secondary voltage
U_{TM}	TM injection electrode voltage
$U_x(t)$	actuation voltage in *x*-axis
U_{x_p}	peak actuation voltage in *x*-axis
U_{x_rms}	RMS actuation voltage in *x*-axis
U_{z_p}	peak actuation voltage in *z*-axis
U_{z_rms}	RMS actuation voltage in *z*-axis
U_{η_p}	peak actuation voltage around *y*-axis (α_η-torque)
U_{η_rms}	RMS actuation voltage around *y*-axis (α_η-torque
$U_\varphi(t)$	actuation voltage around *z*-axis
U_{φ_p}	peak actuation voltage around *z*-axis (α_φ-torque)
U_{φ_rms}	RMS actuation voltage around *z*-axis (α_φ-torque)
$\delta U/U$	relative voltage amplitude fluctuation
$\lvert\partial U_{BR}/\partial\Delta C\rvert$	capacitance to bridge voltage gain (voltage to capacitance gradient)
$\lvert\partial U_O/\partial\Delta C\rvert$	capacitance to TIA voltage gain (voltage to capacitance gradient)
u_{AMP}	op-amp voltage noise
u_{FET}	JFET voltage noise
u_{TH-RDS}	equivalent voltage noise due to JFET r_{DS} thermal noise
u_{TH-ZBR}	equivalent voltage noise due to bridge impedance thermal noise
u_{TH-ZFB}	equivalent voltage noise due to TIA feedback impedance thermal noise
Δu_x	average electrode stray DC voltage imbalance
v	turn-to-turn separation in a winding
W	bandwidth of each sideband of the modulated signal
w	weighting coefficient
X	skin depth factor
x	TM displacement from center in *x*-axis
$x_{1,2}$	*x*-position outputs of two sensing channels
x_{BR0}	*x*-position equivalent of the sensing bridge offset
x_{BR0_C}	*x*-position offset due to asymmetry of bridge capacitors
x_{BR0_K}	*x*-position offset due to transformer coupling asymmetry
x_{BR0_L}	*x*-position offset due to transformer inductance asymmetry
x_{BRS}	*x*-position equivalent of the sensing bridge output (sensing signal free of offset)
x_{comb}	combined *x*-position output
$x_n, x_{n1,2}$	*x*-position RMS noise of two sensing channels
x_{n-comb}	*x*-position RMS noise of combined output
Δx	TM to spacecraft residual jitter (position)
$Z_{a1,a2}$	actuation low-pass filter impedance of channel 1, 2
Z_{BR}	sensing bridge output impedance
Z_{FB}	TIA feedback impedance
Z_{IN}	TIA input impedance
α	torque
$\alpha, \alpha_e, \alpha_F$	initial, effective and relative temperature coefficients
α, β	coefficients of the denominator of the TIA transfer function
α_{η_max}	maximum torque around *y*-axis
α_{φ_max}	maximum torque around *z*-axis

δ	loss angle; skin (effect) depth
ε_0	permittivity of free space
μ, μ_i, μ_e	relative, initial and effective permeability
μ_0	permeability of free space; magnetic field constant
$\Delta\mu_i$	initial permeability variation
μ_r	relative magnetic permeability
$\bar{\mu}, \mu_S', \mu_S''$	relative complex, real (inductive) and imaginary (loss) permeability
ξ	damping constant of the second-order filter
$\xi_{3,4}$	damping constants of $NG(s)$
ρ	resistivity
τ	time constant
ω	angular frequency
ω^2	gravitational stiffness
ω_0	angular resonant (carrier) frequency
$\lvert\omega_{DF}^2\rvert$	DFACS control gain
ω_{LF}	angular (low) frequency
ω_{LP}	angular frequency of the low-pass filter
ω_p, ω_p^2	parasitic coupling
ω_{SR}	self-resonant angular frequency of a winding

Chapter 1
INTRODUCTION

The dissertation aims to provide development guidelines for electronics closely related to the control of reference body used in the detection of gravitational waves. To set a context for the electronics development, an overview of gravitational waves and a short description of planned space missions are given below. The chapter then elaborates on previous work in related fields and on the main goals of the dissertation. The sequence of the dissertation is then explained along with the necessity of the required phases. The main contribution of the dissertation is stated at the end of the chapter.

1.1 Gravitational Wave Detectors

Gravitational waves were predicted by A. Einstein as a consequence of his general theory of relativity [1], [2]. Based on that theory, gravitational waves are generated by accelerated masses, propagate across the universe at the speed of light, and cause distortions in space time curvature.

Up to now, gravitational waves have never been directly observed, due to the weakness of gravitational interactions and the large distance from their sources. Nevertheless, their existence has been indirectly proved by the observation of the binary pulsar PSR 1913+16, discovered by R. A. Hulse and J. H. Taylor. They found that the energy loss of the pulsar was exactly equal to the expected energy loss due to the emission of gravitational waves [3], [4]. For this discovery, they won the Nobel Prize in 1993 [5].

Direct detection of gravitational waves has long been sought, since it would not only confirm the theory of general relativity, but also open up a new branch of astronomy, "gravitational wave astronomy." This would complement electromagnetic telescopes and neutrino observatories and thus provide a new way to observe the universe.

1.1.1 Observation of Gravitational Waves

Joseph Weber pioneered the effort to detect gravitational waves in the 1960s through his work on resonant mass bar detectors [6]. By the 1970s, scientists, including Rainer Weiss, realized the applicability of laser interferometry to gravitational wave measurements [7].

Since then, several experiments, based on acoustic resonators and km-sized interferometers, have been developed and built on Earth in order to detect gravitational waves from ~ 10 Hz – 100 Hz up to the kHz frequency range. Some well-known operational ground-based gravitational wave detectors are: Geosynchronous Earth Orbit (GEO 600) in Germany, Laser Interferometer Gravitational Wave Observatory (LIGO) in the USA, Variability of Irradiance and Gravity Oscillations (VIRGO) in Italy and TAMA 300[1] in Japan. Although only gravitational-wave signals in the frequency range of ~ 10 Hz to ~ 1 kHz can be distinguished from Earth strain signals (< 1 Hz), a long-term stability of the detector is affected by Earth strain fluctuation at low frequencies, e.g., during earthquakes. For this reason, Earth based gravitational wave detectors usually have feedback circuits to compensate for such disturbances.

[1] TAMA stands for the name of a district around the National Astronomical Observatory of Japan (in Tokyo)

Gravitational waves are generated by various astrophysical bodies, but due to the large distance from Earth, their amplitude is very small. The relative strain or the gravitational wave amplitude, with its symbol "*h*," is in the range roughly between 10^{-24} and 10^{-20}. Strain sensitivities from a few times 10^{-20} to below 10^{-21} were hard to imagine a decade ago, but are now achievable[2]. There has been significant development toward a next generation of detectors, such as the Advanced LIGO in the US and the Large Cryogenic Gravitational Telescope (LCGT) in Japan, which promise a dramatic leap in range [8].

Laser Interferometer Space Antenna (LISA) will be the first spaceborne, low frequency gravitational wave detector [9], which will be a good complement to LIGO and other similar devices on the ground. The performance of such Earth-based observatories is usually limited by Earth noises. Furthermore, their size allows only the detection of gravitational waves generated by a limited set of sources at relatively high frequencies. Compared with such Earth-based observatories, LISA will observe the gravitational waves in a different gravity spectrum. The goal of this mission, jointly developed by the European Space Agency (ESA) and the National Aeronautics and Space Administration (NASA), is to detect gravitational waves emitted by galactic sources, e.g., binary stars, and waves emitted by cosmological sources, e.g., massive black holes. The frequency range that LISA will observe is from 0,1 mHz to 0,1 Hz, which is impossible to detect by Earth-based observatories.

The LISA gravitational wave detector is a constellation of 3 satellites in heliocentric orbits. The orbits are adjusted so that the three spacecrafts maintain an equilateral triangle formation with a 5×10^6 km side (Figure 1-1). This satellite formation follows the Earth's orbit with approximately a 20º angle and thus makes observations of the whole universe during one year. The Test Mass (TM) is the core of the inertial (gravitational reference) sensor of the gravitational wave detector. The TM should be in pure geodesic motion - free fall - so that its movement can represent the effect of a gravitational wave. Each spacecraft (Figure 1-2) contains a pair of TMs of approximately 2 kg and a pair of laser transmitters / receivers. The operational principle of LISA is based on laser ranging of TMs that are in pure geodesic motion. Each TM is the end-mirror of a single arm-laser interferometer in which the other end-mirror is on one of the other two spacecrafts. The triangular formation with three single-arm interferometers reconstructs two semi-independent Michelson interferometers, with one arm rotated by 60º and one common arm. Each Michelson interferometer measures the difference of its arm lengths so that the gravitational waves can be detected as relative variations of the two optical paths.

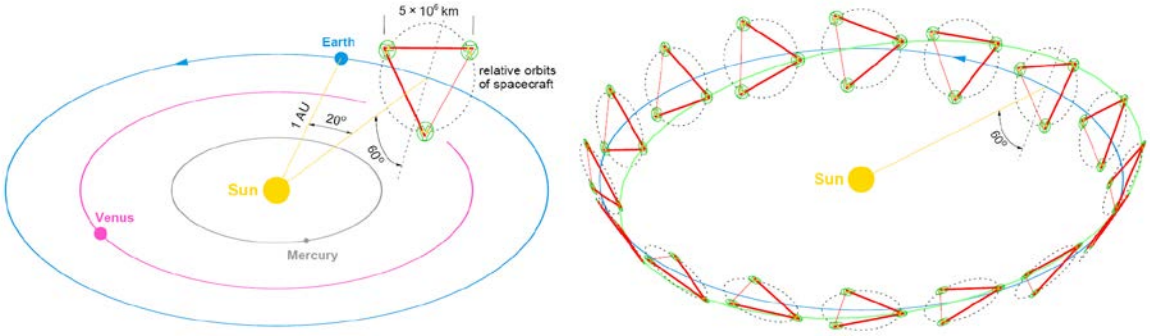

Figure 1-1 LISA satellites in an equilateral triangle formation (drawing not to scale). One 2-arm Michelson interferometer is highlighted to show its annual rotation. The green line shows the trajectory of one spacecraft

[2] The 10^{-21} gravitational wave strain ($h = 2\,\frac{\delta L}{L}$) would change the mean distance metrics (L) between the Earth and the Sun (150×10^9 m) by a value (δL) roughly the size of a hydrogen atom (50×10^{-12} m).

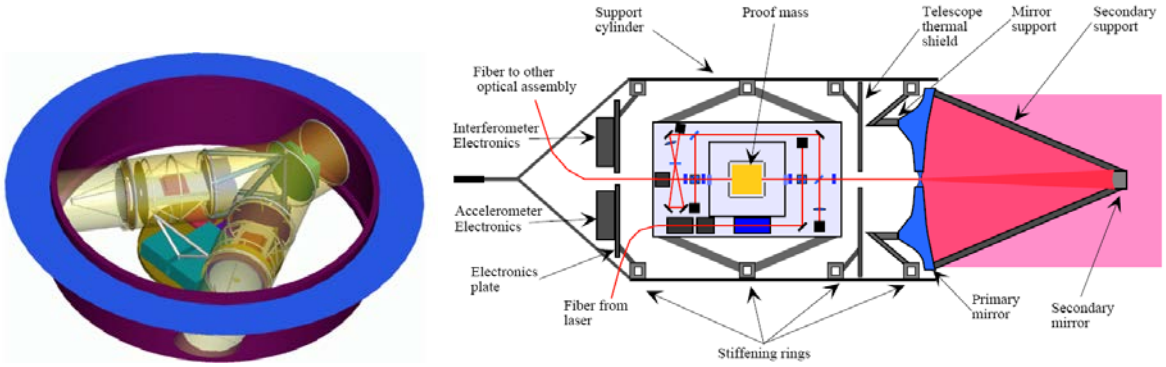

Figure 1-2 LISA spacecraft with top lid removed to show the Y-shaped assembly. Each assembly encloses one TM (also called proof mass) and an electro-optical system

To ensure pure geodesic motion, it is necessary to suppress all external and internal force disturbances on the TMs. This means that the TMs must have no mechanical contact to the spacecraft. Since forces may depend on the position of the TMs within the spacecraft, the spacecraft position must be kept as fixed as possible with respect to the TMs.

To fulfill both of these seemingly conflicting requirements, the spacecraft must actively follow the TM located inside it in a closed loop control scheme maintained by the Drag-Free Attitude Control System (DFACS). In this control concept, the position of the TM, relative to some nominal origin, is measured by means of a Gravitational Reference Sensor (GRS). A high gain control loop of the DFACS then tries to null this error signal by forcing the spacecraft to follow the TM. In order to produce the necessary force on the spacecraft, the control loop drives a set of micro-thrusters.

1.1.2 Demonstration of Technology for a Spaceborne Detector

LISA strain sensitivity goal is $S_h^{1/2} \approx 4 \times 10^{-21}/\sqrt{\text{Hz}}$ around 3 mHz with the noise increasing at both ends of the band (Figure 1-3).

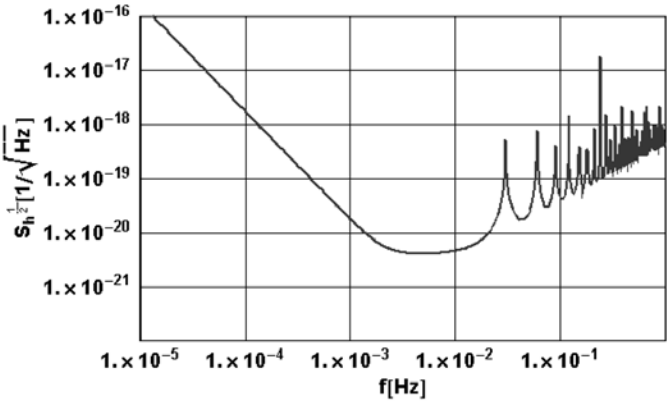

Figure 1-3 LISA strain sensitivity goal of $S_h^{1/2} \approx 4 \times 10^{-21}/\sqrt{Hz}$ around 3 mHz. Sensitivity is reduced at higher frequencies, i.e., to gravitational waves with shorter wavelengths, due to finite laser light travel time and long LISA arms. At lower frequencies, the noise curve rises because of the effect of spurious forces on the test masses

On the LISA mission, achieving the required pure geodesic motion of the TM at the acceleration noise level of $3 \times 10^{-15}\ \text{ms}^{-2}/\sqrt{\text{Hz}}$ and frequency of 0,1 mHz will be a challenging technological objective. In order to reduce the risk of not achieving this objective, both ESA and NASA are pursuing an in-flight test of the relevant technology, namely, the LISA Technology Package (LTP) on board the LISA Pathfinder (LPF)

spacecraft, which is planned for launch in 2013. The goal of the test is to demonstrate geodesic motion with one order relaxation of the LISA requirement, i.e., the acceleration noise level of 3×10^{-14} $\mathrm{ms}^{-2}/\sqrt{\mathrm{Hz}}$ instead of 3×10^{-15} $\mathrm{ms}^{-2}/\sqrt{\mathrm{Hz}}$, and the lower corner frequency of 1 mHz instead of 0,1 mHz (Figure 1-4).

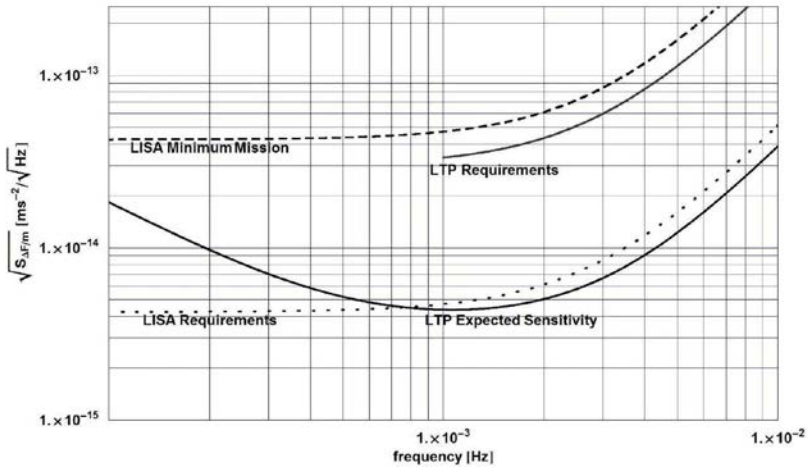

Figure 1-4 Required and projected LISA and LTP acceleration sensitivities in the frequency band from 0,1 mHz to 10 mHz

The contribution of NASA has been reduced during the LPF development from the complete spacecraft Disturbance Reduction System (DRS) to only a set of spacecraft micro-thrusters and related control software.

The aim of ESA is to fly the LPF core sub-assembly, the LTP, in order to demonstrate the possibility of achieving geodesic motion of TMs with accuracy relevant to LISA. Unlike on the LISA mission, only one spacecraft will be flown in LPF with two TMs as part of a single laser interferometer. Also, the distance between the TMs in LISA is five kilometers, whereas on the LPF spacecraft it is only 37 cm (Figure 1-5).

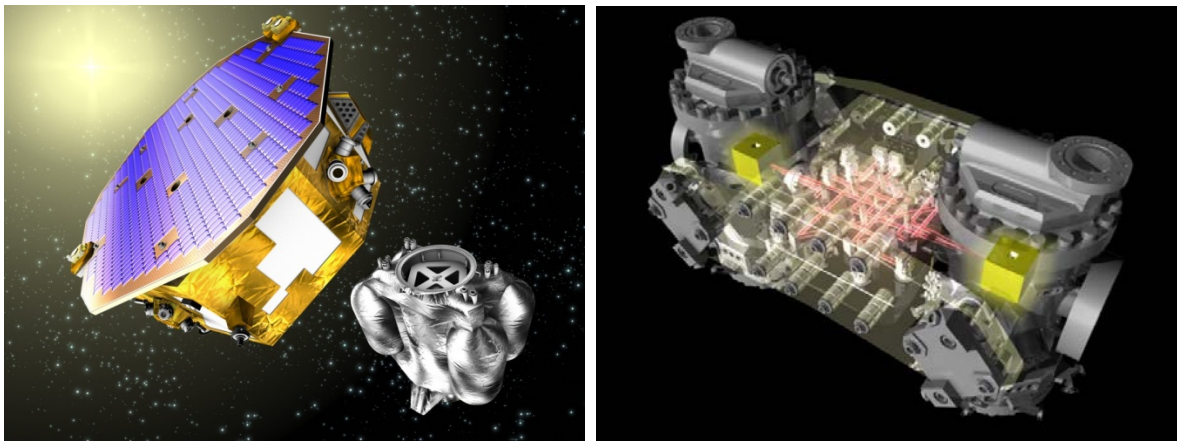

Figure 1-5 LPF spacecraft composite and the LISA Technology Package of the LPF spacecraft. Two TMs are the core of the inertial sensor and are protected in their vacuum enclosures, separated by 37 cm. The optical bench with laser interferometers is located in between two vacuum enclosures, while the electronics of the inertial sensor (not shown) is located on the spacecraft shear walls away from the core assembly to reduce thermal influence on the sensor

Much like in LISA, two TMs are tracked optically by a laser interferometer. Their attitude against spacecraft is sensed and controlled by an Inertial Sensor (IS) subsystem. The micro-thrusters control the spacecraft via DFACS software to follow one TM. The core of the IS subsystem is the sensor itself (Figure 1-6), consisting of two TMs, each inside own vacuum enclosure, surrounded by 12 sensing / actuation electrodes and TM capture / release electro-mechanical devices. Once released, the position of each TM can be measured and controlled via these electrodes by the Inertial Sensor Front-End Electronics (IS-FEE).

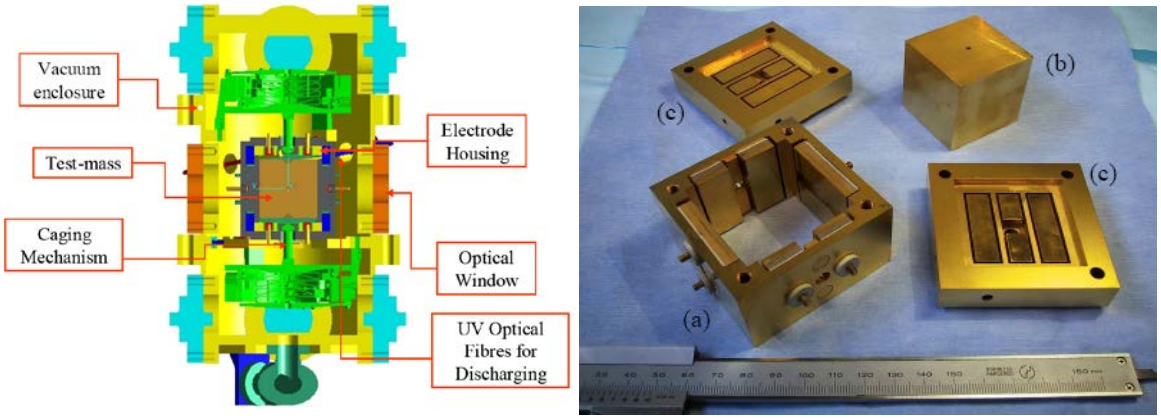

Figure 1-6 Proper sensor of the Inertial Sensor subsystem consists of the electrode housing (a, c) with incorporated electrodes and the TM (b) in its center

Due to short interferometer arm length, LTP cannot detect gravitational waves. However, this minimal instrument is deemed to contain the essence of the technology and construction procedures needed for LISA and thus to demonstrate its feasibility. Once in orbit at the Lagrange point L1[3] (Figure 1-7), the residual differential acceleration noise of the TMs will be measured. The sources of this noise originating from the residual coupling with the spacecraft will be highlighted, measured and eventually suppressed using electric fields. Noise sources due to fluctuations of some physical parameters like magnetic fields or temperature gradients will be measured to identify the transfer function of the corresponding differential TM acceleration fluctuations with respect to these sources. Therefore, the LTP carries magnetic coils, heaters and sensors (magnetometers and thermometers) to induce and measure these physical parameters for the transfer function identification. Based on the transfer functions, the contributions of these noise sources can be suppressed by according counter fluctuation, and thus the residual acceleration noise could eventually be decreased.

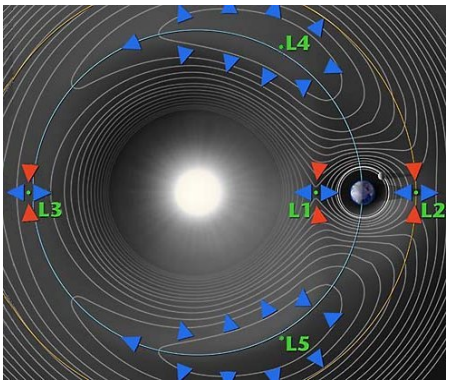

Figure 1-7 Lagrange points, L1 to L5

[3] Lagrange point L1 is an orbital position between the Earth and the Sun where the combined gravitational pull of these two bodies balances in a such a way that the satellite stays stationary against the Earth when orbiting the Sun

The charged particle flux, due to cosmic rays, will be continuously monitored by a particle detector. This flux will accumulate charge on each TM, which will be measured using the TM electrostatic actuation and TM position sensing electronics. The continuous TM discharge using ultra-violet lamps and voltages on actuation/sensing electrodes will try to reduce unwanted TM accelerations caused by this charge.

The LTP in-flight test campaign will last several months, during which two TMs will be placed in "pure-like" geodesic and controlled motion that will allow verification of the noise model and technology readiness for LISA.

1.1.3 Inertial Sensor Front-End Electronics

The LTP contains two TM position sensing sub-systems; one is an electro-optical sub-system based on laser interferometry, and the other is a capacitive sub-system based on electrodes surrounding TMs and the according sensing electronics. The electro-optical sub-system is used to measure the relative position between two TMs in picometer precision along the main measurement axis. The capacitive sub-system is part of the IS-FEE sub-system used to measure the absolute position of TMs against the spacecraft in nanometer precision along all axes. In addition to the electronics necessary for displacement and attitude measurement, i.e., TM sensing, the IS-FEE also includes displacement and attitude control, i.e., TM actuation.

In order to achieve the required performance, both sensing and actuation electronics should not generate stray noises larger than $1/10^{th}$ of the required TM acceleration sensitivity levels. This is challenging not only in terms of circuit design and electronic components selection, but also in terms of measurement and verification.

In a sensing circuit, the required capacitance sensitivity level is $10^{-6}\mathrm{pF}/\sqrt{\mathrm{Hz}}$ ($1\ \mathrm{aF}/\sqrt{\mathrm{Hz}}$), which is equivalent to about $2\ \mathrm{nm}/\sqrt{\mathrm{Hz}}$. In an actuation circuit, the required actuation waveform amplitude stability is $2\ \mathrm{ppm}/\sqrt{\mathrm{Hz}}$. These requirements are particularly difficult to achieve below frequencies of 10 mHz. Also, using common electrodes for sensing at nanometer scale and actuation with voltages larger than 100 V are difficult to implement. Furthermore, a low TM excitation level should be used to prevent stray accelerations, which requires design with a very low sensing noise floor. Therefore, similar circuits from commercial projects are not qualified for use and the design itself presents a considerable technological challenge. In addition, most of the commercially available electronic components cannot be used in a space environment, which makes design difficult in terms of optimizing performance, size, mass and power.

The measurement and verification of the design is not an easy task. In general, the noise performance of electronics components is not very well specified below 1 Hz. Characterizing the performance at a very low frequency requires that the test environment be under tight control to limit thermal drifts, which mix with the $1/f$ flicker noise and mask the real electronics performance. Therefore, special measurement and verification methods need to be studied.

Without going into too much detail at this point, the main IS-FEE functions can be divided as follows:

- TM biasing (excitation) with AC (100 kHz) voltage via injection electrodes for TM displacement and attitude sensing
- TM displacement and attitude sensing in 6 degrees of freedom using 6 pairs of sensing electrodes

- TM biasing with AC (< 300 Hz) voltages via actuation electrodes[4] for TM displacement and attitude control
- TM biasing with DC and low frequency (< 0,1 Hz) voltages via actuation electrodes for cancelling TM stray voltages and also for TM charge measurement and discharge
- Acquisition of sensing voltages, conversion to digital data and serial interface with the spacecraft computer to provide inputs for the spacecraft control (DFACS)
- Acceptance of digital outputs from the DFACS over serial interface, conversion to analog voltages and their conditioning for the actuation electrodes

A simple block diagram of the IS-FEE subsystem is shown in Figure 1-8. It consists of the cold-redundant (completely duplicated) Sensing and Actuation Unit (SAU), Sensor Switching Unit (SSU), Power Conditioning Unit (PCU) and a cable harness. All previously listed main IS-FEE functions are enclosed within each of the SAUs. The SSU serves to connect one of the two redundant SAU electronics to the TM electrodes and the PCU provides necessary secondary stabilized power supply voltages generated from the primary spacecraft voltage.

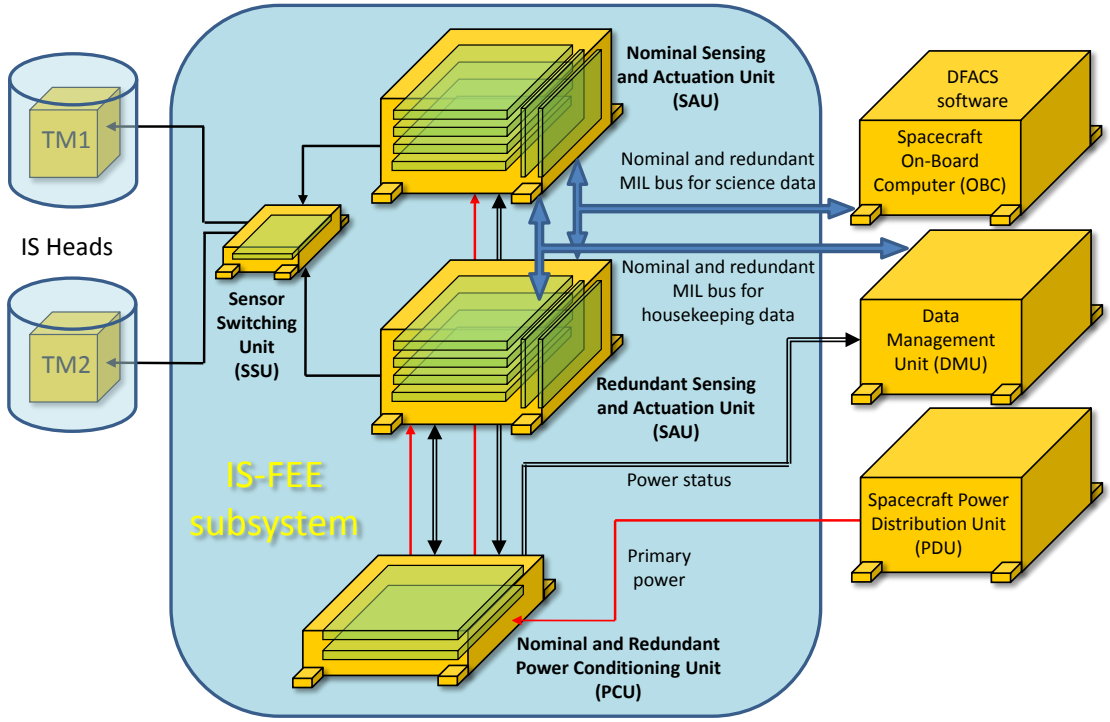

Figure 1-8 Block diagram of the Inertial Sensor Front-End Electronics

The location of the IS-FEE subsystem on the LPF spacecraft is shown in Figure 1-9.

[4] Same electrodes are used for the sensing and actuation function

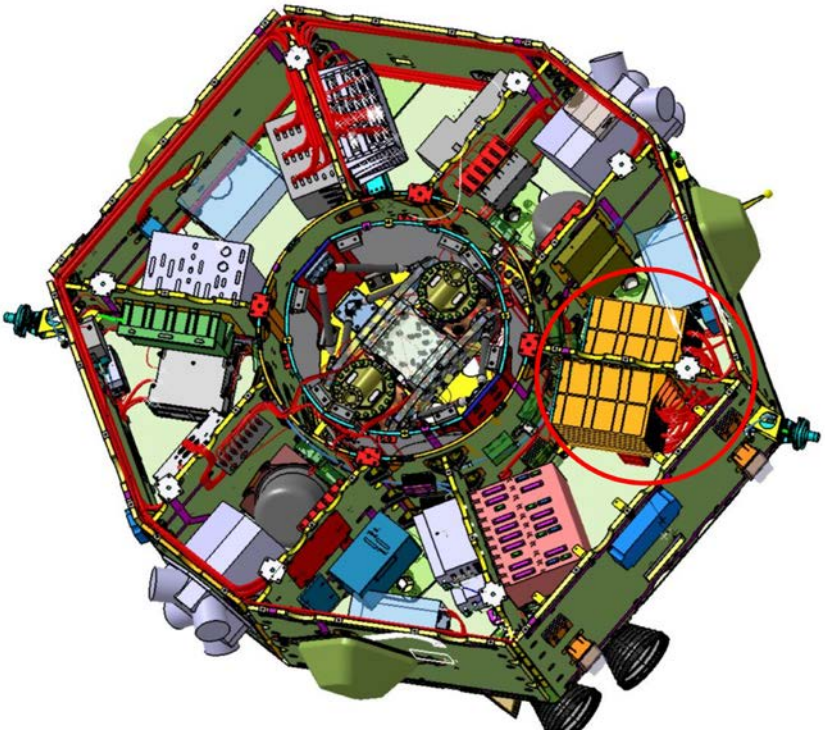

Figure 1-9 Location of the Inertial Sensor Front-End Electronics on the LPF spacecraft is indicated by the red circle. The LTP core assembly is located in the center of the spacecraft

1.2 Dissertation Goal

The goal of the dissertation is to present an IS-FEE design that would fulfill the top-level requirements imposed by the LPF mission. Therefore, a work covered by this dissertation has been launched aiming to fulfill the following general objectives:

- Analysis of top-level physical requirements and their conversion into electronics requirements
- Definition of main design drivers and technological challenges
- Evaluation of possible design options, including those covered by previous developments
- Verification of selected designs by testing on hardware before or in parallel with the start of the (semi-independent) IS-FEE development by the industrial contractor
- Transfer to the industry the acquired know-how, including a summary of test results, conclusions and lessons learnt

Even though the author performed substantial work on the supervision of industrial development and the assessment of the flight electronics design, this work is not included in this dissertation.

1.3 Previous Developments

The existing work on LTP and LISA, particularly on the design of the Inertial Sensor (IS) in LTP, also called the Gravitational Reference Sensor (GRS) in LISA, was initialized by the Department of Physics of the University of Trento (UTN). The development of the IS core assembly - TM with its sensing / actuation electrodes, and the initial study of the associated front-end electronics, was performed by the Office National d'Etudes et de Recherches Aérospatiales (ONERA). ONERA is experienced in the development of space electrostatic

accelerometers for Earth observation, which were used for the Gradiometer (GRADIO) and Accéléromètre Spatial TRiaxial Electrostatique (ASTRE) missions [10].

Several papers and doctoral theses concerning the IS development [11], [12] have been published by these two institutes, and they can be considered the foundation of the final mechanical design of the IS. The sensors and electronics from ONERA, designed to fulfill the requirements for observation of Earth gravity, did not have the required level of performance for LISA. Hence, it was clear that a different sensor had to be developed for LISA, namely, Capacitive and Electrostatic Sensitive Accelerometer Reference (CAESAR), as proposed in [13]. In these publications, key parameters for achieving the required sensitivity level are specified, such as the TM size, the size of the gaps between the TM and the surrounding electrodes, the size of the electrodes and the selection of material. These are the prerequisites for the IS-FEE development.

Since neither LISA's nor LTP's performance can verified on the ground because of the Earth's strong gravity, ground verification relies mostly on the measurements of the key parameters of the instrument's noise model [14]. A torsion pendulum test-bench was built in 2001 and is operating at UTN [15] to establish an upper limit for ground verification of residual accelerations on the TM. The achieved upper limit has relaxed the acceleration magnitude level by two orders compared with the LISA requirement, i.e., the acceleration noise level of $3 \times 10^{-13}\ \mathrm{ms}^{-2}/\sqrt{\mathrm{Hz}}$ instead of $3 \times 10^{-15}\ \mathrm{ms}^{-2}/\sqrt{\mathrm{Hz}}$. These residual accelerations are the result of all parasitic forces that act on the TM, e.g., electrostatic, electromagnetic and thermal, pressure effects, etc. In this instrument, a hollow version of the TM hangs on the torsion fiber of the pendulum so that it can freely move in a horizontal plane, which simulates the flight conditions, i.e., the absence of gravity. The UTN's work included the preliminary design of the core circuits of the sensing and actuation electronics [16] for operating the torsion pendulum. This was the basis for further development to fully achieve the required LTP performance.

In 2003, the inertial sensor development was divided into Italian and Swiss contribution. Then, the proper mechanical sensor – the TM and its electrode enclosure are developed in Italy under close supervision of UTN, and the sensor electronics – the IS-FEE are developed in Switzerland under the supervision of ETHZ.

The previous work on mechanical design was about sensing geometry, i.e., about the variation of capacitance between the TM and its electrodes, which can be achieved by gap variation or by area variation. Area variation geometry was suggested by ONERA for the CAESAR instrument because it could generate lower parasitic stiffness, i.e., the back-action force exerted on the TM [17]. This design was asymmetric, i.e., with area variation geometry along the most sensitive *x*-axis, which is in line with the laser interferometer beam measuring the distance between two TMs, and with gap variation geometry along the other axes. In the end, the gap-sensing electrode design was chosen as a baseline [18], due to the requirement of having large gaps to reduce un-modeled surface forces and obtaining equal performance for all degrees of freedom to suppress possible cross-talk effects.

The development of sensor electronics was concentrated mostly on the transformer bridge and the preamplifier circuit, which are the core of the TM displacement, i.e., the capacitance detection circuit. In the transformer bridge design, by analyzing the resonant circuit against the non-resonant one [19], it was concluded that both circuits would comply with the level of generated back-action force on TM. In the end, the resonant circuit was chosen as a baseline [20]. Note that the design of IS for LISA differs from the design of a space accelerometer. In LISA, the reduction of all stray forces acting on the TM is the preference at the expense of displacement sensitivity. This is the reason why the baseline for the TM excitation level was

chosen to be relatively low i.e., 0,6 V [18], compared with very sensitive accelerometers where the signal-to-noise ratio is improved with large excitation voltages, e.g., 5 V - 10 V.

The front-end part of the sensing electronics, including the TM excitation oscillator, was built and tested at UTN in order to demonstrate that theoretical calculations could be verified by the working hardware. Several circuits were tested with different performance levels and improving low-frequency sensing noise will constitute future work [16]. In particular, the importance of careful cabling and the avoidance of ground loops have been recognized as dominating factors for achieving performance at low frequencies.

Previous work on TM actuation electronics was related to the top-level control loop design of the LPF spacecraft (DFACS) or the spacecraft control in ONERA accelerometers. The simple actuation electronics were built at UTN for the purpose of actuating the TM in the torsion pendulum test bench [21]. However, the stability of this actuation electronics, which was compatible with the torsion pendulum test-bench and laboratory environment stray accelerations, could not satisfy the requirements of LISA or LTP. Also, the design of the electrostatic actuation circuit, the Drive Voltage Amplifier (DVA) used in Earth-based accelerometers [22], had to be modified to be compatible with LISA. In particular, larger TM gaps require larger actuation voltages to generate the same force, and very large voltages of more than 100 V had to be provided for the initial stabilization of the TM after its release. The very stable actuation amplitude generation had to be analyzed, modeled and finally verified on hardware. Furthermore, different actuation schemes had to be evaluated for suitability with respect to noise performance, crosstalk and other engineering parameters.

Although previous work provided an important contribution to the analysis of the technological boundaries for the required performance of the electronics, it did not include all necessary circuits in the analysis, did not provide detailed modeling and did not achieve full performance in all aspects. Hence, the complete and professional electronics that can achieve full performance had to be built. Also, comprehensive analysis of all noise sources in the circuit should be provided to investigate performance margins. Furthermore, an analysis of availability and suitability of commercial and space-qualified electronics components for the flight hardware should be given to guide the industrial development.

In this dissertation, the design of the IS sensing and actuation electronics in LTP will be studied. The focus will be on the sensing transformer and the preamplifier design, which are the dominating sources of the sensing noise. Different engineering techniques concerning the transformer manufacturing design will be studied and checked to achieve required winding symmetry responsible for the TM displacement offset, which is another challenging requirement. The stability of the TM excitation voltage oscillator and the TM actuation voltages will be another major topic, not only in design but also in verification.

1.4 Sequence of the Dissertation

The sequence of the dissertation followed in general the objectives listed in Section 1.2. First, an analysis of the top-level requirements for the IS-FEE electronics is given, such as the TM back-action force noise caused by the readout circuit itself and the TM acceleration noise caused by the actuation voltages applied on electrodes around the TM. Besides these main requirements, other requirements, such as sensing offsets and relative stability of actuation voltages, are evaluated as well. After the main design challenges have been identified, the IS-FEE requirements specification document is drafted [23].

Then, possible design solutions for sensing and actuation circuits are investigated, including theoretical analysis, modeling and simulation of circuits using SPICE software - MicroCap and Matlab.

With respect to the selection of electronic components, different IS-FEE design solutions are provided and the influence on performance is pointed out when using space-qualified parts, commercial parts with space heritage and truly commercial-of-the-shelf (COTS) parts. Since the best performance is usually achieved with the COTS and the radiation safe performance only with space-qualified parts made in older technologies, the tradeoff between these two nominally opposing designs is studied.

In order to evaluate the performance, prototype circuits and simulators are built and tested at ETHZ. Appropriate software tools (e.g., LabView) for test instrumentation control and data analysis are used to develop scripts facilitating long autonomous tests for evaluating low-frequency performance. Then, a complete multi-channel sensing and actuation control electronics is built and tested in-house as well as on the torsion pendulum test-bench in zero-like gravity conditions in order to fully evaluate the electronics performance.

At the end of the dissertation, the analysis of the performance and knowledge learnt from this work are summarized for industrial development and future space missions.

1.5 Expected Contribution of the Dissertation

Direct detection of gravitational waves would not only prove the theory of general relativity, but also open up a new branch of astronomy - “gravitational wave astronomy.” This would complement electromagnetic telescopes and neutrino observatories and thus provide a new way to observe the universe. The IS-FEE electronics is one of the core subsystems of the gravitational wave detector and its performance is crucial for the success of the LPF and LISA missions.

Besides this fundamental contribution, which would prove the predicted physical laws and open “doors” for new exploration, the expected scientific contribution of this dissertation is:

- Design and realization of an inertial sensor for LISA that will present the low frequency (0,1 mHz to 0,1 Hz) spaceborne gravitational wave detector
- Development and realization of crucial circuits in the field of position sensing and actuation of the TM with challenging performance specifications (exceptionally low noise at low frequencies)
- Search for new ideas and solutions during realization of circuits with the required performance level for capacitive sensing and electrostatic actuation, as existing knowledge is not sufficient to achieve all requirements
- Upgrade of existing measurement and verification methods with new ideas and new simulators
- Establishment of a firm foundation for flight electronics development and future development of the LISA mission with requirements ten times as stringent

Chapter 2
POSITION SENSING OF TEST MASS

The Test Mass (TM) is the core of the Inertial Sensor (IS) in LTP or the Gravitational Reference Sensor (GRS) in LISA. It is a cube with 46 mm sides, roughly of 2 kg mass and made of Au/Pt alloy (70% / 30%) to minimize magnetic susceptibility and residual magnetic moment, and achieve high density to minimize the acceleration noise for a given force noise [12].

The TM (Figure 2-1) is surrounded by electrode housing holding twelve sensing / actuation electrodes (two facing each TM side), which form six pairs of sensing electrodes. Thus, each pair of the sensing electrodes consists of a front and rear electrode relative to the TM.

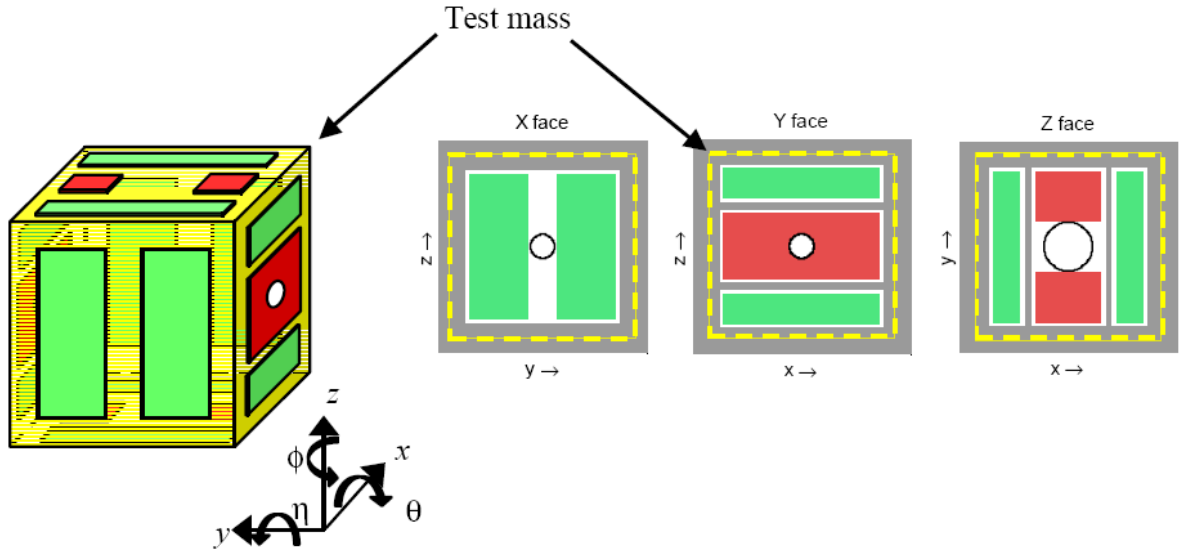

Figure 2-1 TM (yellow) with sensing/actuation (green) and injection (red) electrodes. Holes on X and Y faces are used for the laser beam to pass and reflect from the TM, while holes on Z faces are for the caging mechanism that holds the TM until spacecraft arrives at the operating site. The largest gap of 4 mm is between the TM and the X face electrodes, i.e., along the main X measurement axis, being also the laser beam axis. When the TM is in the center of the electrode housing this electrode geometry sets sensing capacitance of ≈ 1,15 pF along X-axis

The readout circuit scheme, in principle shown on Figure 2-2, was settled very early during mission development. It is based on a capacitive-inductive resonant bridge, with the capacitive (C_{p1}, C_{p2}) and inductive components (L_1, L_2) chosen to resonate at a certain frequency. An excitation signal at that frequency is injected on the TM through a set of six injection electrodes, 2+2 on the *Z* faces plus 1+1 on the *Y* faces (Figure 2-1). The level of the injection voltage will be chosen as a tradeoff between the sensing sensitivity, in favor of a higher level for a larger signal-to-noise (S/N) ratio and the sensing back-action force noise on the TM in favor of a lower voltage level for lower force noise.

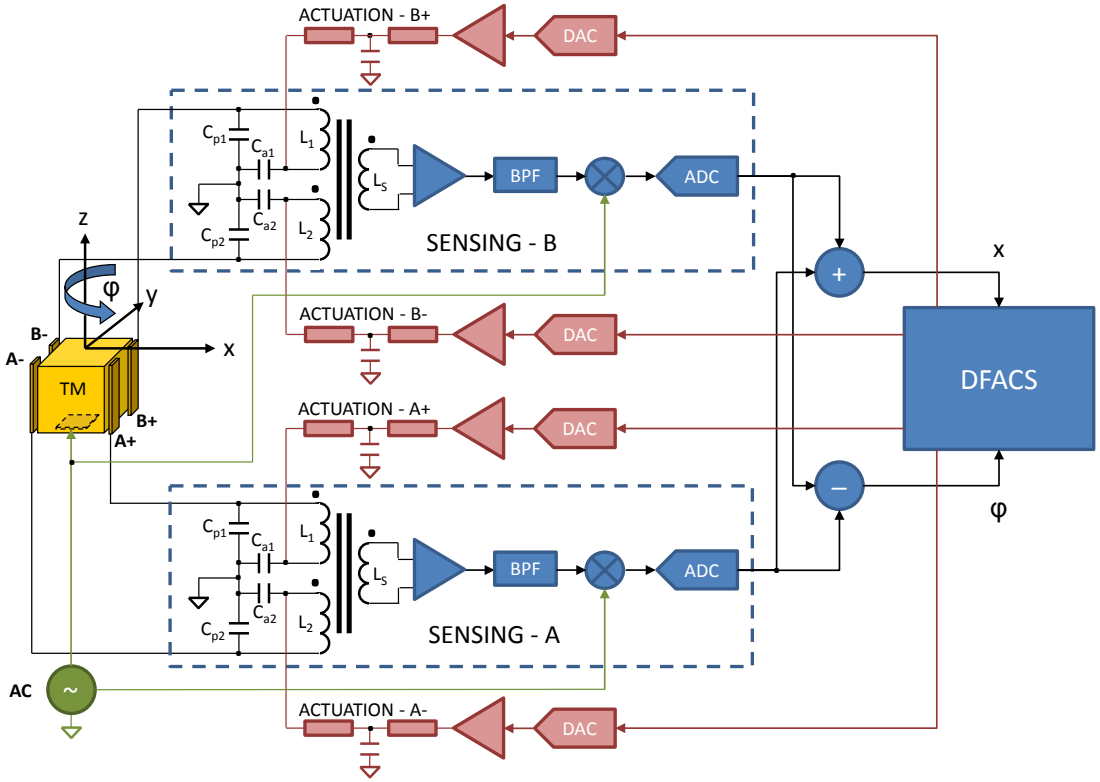

Figure 2-2 The TM position readout circuit for two DOF: displacement along x – axis and rotation around z – axis. The same scheme is implemented for the remaining four DOFs. Injection signal (green) is used to generate currents through the sensing transformers and for demodulation of the resulting AC signal. Actuation electronics is shown with red blocks and sensing with blue ones. The sum of the outputs from two sensing channels is used to calculate the TM displacement and the difference of the outputs, the TM rotation

The movement of the TM inside the electrode housing causes an imbalance of the sensing bridge, i.e., of the currents inside the transformer primary winding L_1 and L_2, which generates differential voltage on the transformer secondary winding L_S. The amplitude of this voltage at injection frequency is proportional to the gain of the sensing circuits and the TM position with respect to the center of the electrode housing. This voltage is amplified, band-pass filtered and only the frequency component in phase with the injection frequency is extracted using synchronous demodulation. This analog signal is finally converted to a digital form by an analog-to-digital converter (ADC).

By linear combination of the six readout channels[5], the selected geometrical configuration of the electrodes provides information on all six Degrees of Freedom (DOFs) of the TM and permits electrostatic actuation on the same DOFs.

The TM translation and rotation measured by the IS-FEE sensing circuits is used by the DFACS to control the LPF spacecraft via the micro thrusters on the main "*x*" measurement axis so that the spacecraft can track the main free-falling TM. The electrostatic actuation is used to control the remaining DOFs of the first TM and all the DOFs of the second TM, since the spacecraft has a limited number of DOFs to control and certainly cannot follow both TMs simultaneously.

[5] The sum of sensing outputs from two neighboring electrode pairs provides the TM translation, while their difference is used to calculate the TM rotation with respect to the center of the electrode housing.

Using a digital-to-analog converter (DAC), the calculated actuation data are converted into analog signals with much lower frequency compared with the sensing frequency. The actuation signals are amplified, low-pass filtered and injected on electrodes via the transformer primary windings. Note that capacitors C_{a1} and C_{a2} on Figure 2-2 are part of the last stage of the actuation low-pass filters and chosen large enough to present a low impedance path for the sensing injection frequency in order to allow simultaneous operation of both sensing and actuation functions. According to the control algorithms of DFACS, voltages applied on electrodes will maintain both TMs along all DOFs centered inside their electrode enclosures.

2.1 Measurement Noise of the Readout Circuit

The sensing bridge is the most critical part of the sensing electronics because it is in direct connection with the sensor. The electronic components that follow the bridge, i.e., the amplifier and the demodulator, can be selected with more freedom. Hence the noise shall be minimized in the bridge before its further amplification.

Initially, a simple model of the bridge will be introduced with the aim of calculating the main characteristics of the capacitance readout circuit, in particular the noise that will set the performance for the capacitance measurement and the equivalent TM position noise.

2.1.1 Sensing Bridge Model

A simplified schematic of the sensing bridge is shown in Figure 2-3. The injection AC voltage U_M is applied on the TM, as shown below located at the connection between capacitors C_1 and C_2, which represent the capacitances between the TM and two surrounding electrodes (front and rear). Actually, the AC voltage is not directly applied to the TM but electrostatically via the injection electrodes, which form injection capacitance between themselves and the TM. Since the TM has additional stray capacitance with respect to the ground and thus it constitutes a capacitive attenuator with the capacitance of the injection electrodes, the AC signal applied on injection electrodes is attenuated on the TM. To simplify the analysis, this capacitive attenuator is not shown and the U_M already represents the voltage on the TM.

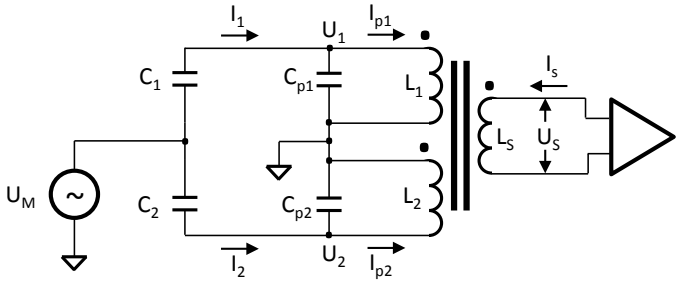

Figure 2-3 Simplified sensing bridge for the purpose of noise calculation

The circuit is an inductive-capacitive bridge in which the differential transformer, with its primary windings L_1 and L_2, is made to resonate with capacitors C_{p1} and C_{p2} at the exact frequency of the input AC signal. The capacitances required for tuning the resonance consists of the lump capacitors of the electronic circuit and the capacitance of the coaxial cable connected between the TM electrodes and the electronics. These capacitances also include the internal stray capacitances of the primary windings.

Two primary windings of the transformer are oriented in such a way that the electromagnetic fields generated by their currents I_{p1} and I_{p2} cancel each other in the transformer core when the TM is at the center of the electrode housing. Hence, the current I_S in the secondary

winding L_S will indicate the TM position from the center position. The preamplifier connected on the bridge output will be analyzed later, and it will be shown that the noise of the sensing bridge alone is the dominating source of the noise. Note that another simplification is made: the capacitors C_{a1} and C_{a2} of the actuation filter shown in Figure 2-2 are here shown as shorts between the primary windings and the ground because they do not significantly influence the noise and present very low impedance at the frequency of the input AC signal.

The sensing bridge is seen by the preamplifier as an equivalent voltage signal $U_{BR}(\omega)$ given by the output circuit response of the bridge, in series with the bridge source impedance $Z_{BR}(\omega)$ as shown in Figure 2-4.

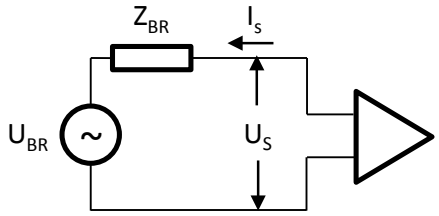

Figure 2-4 Sensing bridge equivalent circuit

In this analysis, this equivalent circuit will be evaluated first, as it will be the basis for the noise evaluation.

2.1.1.1 Sensing bridge output voltage

Using Kirchhoff's circuit laws, the currents through the primary windings of the transformer I_{p1} and I_{p2} in Figure 2-3 can be written as

$$\begin{aligned} I_{p1} &= sC_1\,(U_M - U_1) - sC_{p1}U_1 = sC_1\,U_M - s\big(C_1 + C_{p1}\big)U_1 \\ I_{p2} &= sC_2\,(U_M - U_2) - sC_{p2}U_2 = sC_2\,U_M - s\big(C_2 + C_{p2}\big)U_2 \end{aligned} \tag{2.1}$$

where U_M is the injection voltage at the TM, C_1 and C_2 are the sensing capacitances, and C_{p1} and C_{p2} are the resonance tuning capacitances.

Since the voltages on the transformer windings are all related, U_1 and U_2 are

$$\begin{aligned} \frac{U_1}{n_1} &= -\frac{U_2}{n_2} = \frac{U_S}{n_S} \\ U_1 &= \frac{n_1}{n_S}U_S = U_S \\ U_2 &= -\frac{n_2}{n_S}U_S = -U_S \end{aligned} \tag{2.2}$$

where n_1, n_2 and n_S are the number of turns of the primary and secondary windings, respectively, and are selected to be equal on the LTP project (based on previous development). Substituting U_1 and U_2 in (2.1) with (2.2) the currents through the primary winding are

$$\begin{aligned} I_{p1} &= sC_1\,U_M - s\big(C_1 + C_{p1}\big)U_S \\ I_{p2} &= sC_2\,U_M + s\big(C_2 + C_{p2}\big)U_S \end{aligned} \tag{2.3}$$

Considering the mutual inductances M_{ij} of the transformer, its secondary voltage U_S can be written as

$$U_S = sL_S I_S + sM_{1S} I_{p1} - sM_{2S} I_{p2}$$
$$M_{1S} = K\sqrt{L_1 L_S}\ ,\ M_{2S} = K\sqrt{L_2 L_S} \tag{2.4}$$

where K is the coupling coefficient between windings and L_1, L_2 and L_S are the inductances of the primary and secondary windings of the transformer. In this simple model one can assume that the transformer is fairly ideal, i.e., with the coupling coefficient $K = 1$ and since windings have an equal number of turns, all inductances are equal $L_1 = L_2 = L_S = L$. With these assumptions, (2.4) can be rewritten as

$$U_S = sL\left(I_S + I_{p1} - I_{p2}\right) \tag{2.5}$$

According to Figure 2-4, the voltage signal U_{BR} is equal to the secondary voltage U_S when the secondary circuit is open ($I_S = 0$). In the open circuit condition, the substitution of I_{p1} and I_{p2} in (2.5) with (2.3) gives the secondary voltage as

$$U_S = U_{BR} = \frac{s^2 L(C_1 - C_2)}{1 + s^2 L\left(C_1 + C_2 + C_{p1} + C_{p2}\right)} U_M \tag{2.6}$$

The input capacitances can be written as

$$C_1 = C_0 + \frac{\Delta C}{2}$$
$$C_2 = C_0 - \frac{\Delta C}{2} \tag{2.7}$$

where C_0 is the capacitance with the TM centered between the electrodes and ΔC is the differential sensing capacitance. As tuning capacitances C_{p1} and C_{p2} are nominally equal (C_p), an equivalent resonance tuning capacitance C_{eq} can be defined as

$$C_{eq} = 2\left(C_0 + C_p\right) \tag{2.8}$$

which includes the sensing capacitance C_0. The value of C_0 is negligible compared to C_p.

Substituting (2.7) in (2.6), using relation (2.8) and $s = j\omega$ gives final equation for the bridge voltage source.

$$U_{BR} = U_M \frac{s^2 L}{1 + s^2 L C_{eq}} \Delta C$$
$$U_{BR} = U_M \frac{-\omega^2 L}{1 - \omega^2 L C_{eq}} \Delta C \tag{2.9}$$

From (2.9) important conclusions can be drawn:

- Bridge output voltage reaches its maximum at the resonant frequency set by L and C_{eq}; output voltage is also infinite because it represents the model of an ideal lossless transformer. The real transformer with losses will be modeled in 2.1.1.3
- TM injection voltage U_M acts as a gain factor that can set the S/N ratio
- Bridge output is proportional to the difference of sensing capacitances, which is a good approximation of the TM position only for small TM displacements from the center position

2.1.1.2 Sensing bridge impedance

According to Figure 2-4, the secondary voltage $U_S = 0$ when the secondary circuit is shorted. This condition makes it possible to calculate the bridge impedance $Z_{BR,}$ defined as the ratio between the bridge voltage signal U_{BR} and the bridge (transformer) secondary current I_S

$$Z_{BR} = \left|\frac{U_{BR}}{I_S}\right| \tag{2.10}$$

where the absolute value is taken to eliminate signal sign definition.

In the short circuit condition, the voltages at the transformer primary windings must also be zero according to (2.2) and therefore, (2.3) can be written as

$$\begin{aligned} I_{p1} &= sC_1\, U_M \\ I_{p2} &= sC_2\, U_M \end{aligned} \tag{2.11}$$

Substituting I_{p1} and I_{p2} in (2.5) with (2.11), the short circuit current can be written as

$$I_S = -s\Delta C U_M \tag{2.12}$$

The secondary current is proportional to the TM displacement and the injection voltage on the TM. Finally, substituting the bridge voltage source U_{BR} and the bridge secondary current I_S in (2.10) with (2.9) and (2.12), respectively, gives the bridge source impedance Z_{BR}

$$\begin{aligned} Z_{BR} &= \frac{sL}{1 + s^2 LC_{eq}} \\ Z_{BR} &= \frac{j\omega L}{1 - \omega^2 LC_{eq}} \end{aligned} \tag{2.13}$$

From (2.13) one can similarly conclude that the bridge impedance reaches its maximum at the resonant frequency set by L and C_{eq}. It appears to be infinite only due to the assumption of the ideal and lossless transformer.

2.1.1.3 Real transformer

In the real transformer the winding is not purely inductive and hence, the real inductance L_R of the transformer will include the resistance R_L and the corresponding loss angle δ between the pure reactance $j\omega L$ and the real reactance $j\omega L_{R,}$ as shown in Figure 2-5.

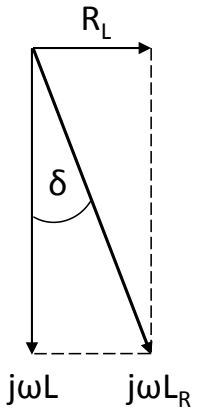

Figure 2-5 Loss angle δ of the real inductor L_R

The loss angle δ can be approximated for small angles with *tan* δ, which can be written as

$$\tan\delta = \frac{R_L}{|j\omega L|} = \frac{R_L}{\omega L} \cong \delta = \frac{1}{Q} \tag{2.14}$$

where the inverse of the loss angle is the inductor quality factor *Q*. Figure 2-5 and (2.14) allow the real inductance to be written in the following form

$$\begin{aligned} sL_R &= R_L + sL \\ L_R &= L + \frac{R_L}{s} = L - j\frac{R_L}{\omega} = L\left(1 - j\frac{R_L}{\omega L}\right) = L(1 - j\delta) \end{aligned} \tag{2.15}$$

After replacing ideal inductances L in (2.9) and (2.13) with L_R from (2.15), the real transformer bridge output voltage and impedance can be rewritten as

$$\begin{aligned} U_{BR} &= U_M \frac{sR_L + s^2L}{1 + sR_LC_{eq} + s^2LC_{eq}}\Delta C \\ U_{BR} &= U_M \frac{-\omega^2L(1 - j\delta)}{1 - \omega^2LC_{eq}(1 - j\delta)}\Delta C \end{aligned} \tag{2.16}$$

$$\begin{aligned} Z_{BR} &= \frac{R_L + sL}{1 + sR_LC_{eq} + s^2LC_{eq}} \\ Z_{BR} &= \frac{j\omega L(1 - j\delta)}{1 - \omega^2LC_{eq}(1 - j\delta)} \end{aligned} \tag{2.17}$$

By combining (2.16) and (2.17), U_{BR} can be rewritten in a simple form as

$$U_{BR} = j\omega Z_{BR} \cdot \Delta C \cdot U_M \tag{2.18}$$

Plots of the bridge output voltage and impedance are shown in Figure 2-6 and Figure 2-7, respectively. At the bridge resonant frequency, the real part of the bridge voltage and the imaginary part of the bridge impedance are equal to zero. At this frequency both the bridge output voltage and impedance achieve maximum.

To calculate the resonant frequency, one must first split the bridge impedance (2.17) into the real and imaginary parts and then find a solution for frequency at which the imaginary part is zero.

$$Z_{BR} = \omega L \frac{\delta + j\left[1 - \omega^2LC_{eq}(1 + \delta^2)\right]}{1 - \omega^2LC_{eq}\left[2 - \omega^2LC_{eq}(1 + \delta^2)\right]} \tag{2.19}$$

$$\Im[Z_{BR}] = 1 - \omega^2LC_{eq}(1 + \delta^2) = 0 \tag{2.20}$$

The solution for (2.20) is the resonant frequency of the bridge, which can be written as

$$\omega_0 = \frac{1}{\sqrt{1 + \delta^2}}\frac{1}{\sqrt{LC_{eq}}} = \frac{Q}{\sqrt{1 + Q^2}}\frac{1}{\sqrt{LC_{eq}}} \tag{2.21}$$

For the assumed bridge quality factor $Q > 100$, (2.21) can be simplified to

$$\omega_0 \cong \frac{1}{\sqrt{LC_{eq}}} \tag{2.22}$$

Figure 2-6 and Figure 2-7 are given for an exemplary transformer bridge with the circuit parameters given in Table 2-1.

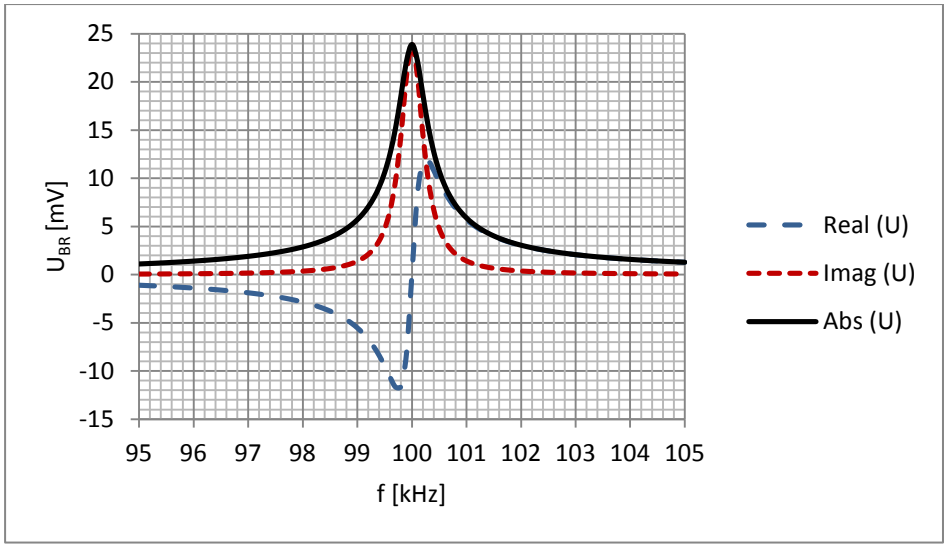

Figure 2-6 Bridge output voltage for C_{eq} chosen to resonate the bridge at 100 kHz and for circuit parameters from Table 2-1

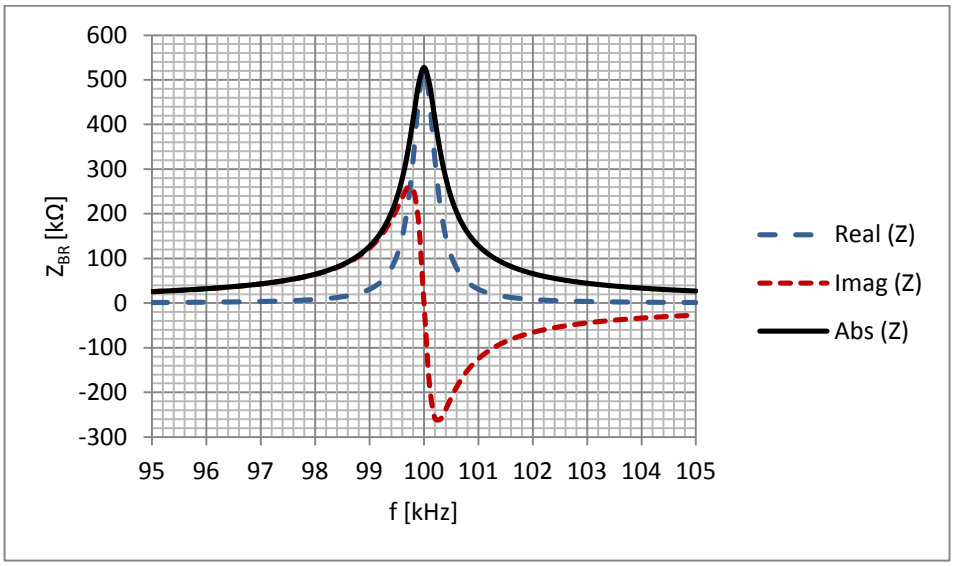

Figure 2-7 Bridge output impedance for C_{eq} chosen to resonate the bridge at 100 kHz and for circuit parameters from Table 2-1

Table 2-1 Parameters of an exemplary sensing bridge

Parameter	Description	Value
U_M	TM peak injection voltage (100 kHz)	0,6 V
ΔC	Differential sensing capacitance for TM out off center	0,12 pF
C_0	Nominal capacitance for centered TM	1,15 pF
C_p	Tuning capacitance per bridge arm	300,39 pF
C_{eq}	Equivalent capacitance $2(C_0 + C_p)$	603,08 pF
L	Transformer winding inductance	4,2 mH
Q	Transformer quality factor	200

The bridge voltage and impedance at the resonant frequency can be calculated by substituting ω in (2.16) and (2.17) with (2.21).

$$U_{BR}(\omega_0) = j\frac{Q}{C_{eq}}\Delta C \cdot U_M$$
$$Z_{BR}(\omega_0) = \omega_0 L\frac{1+Q^2}{Q} \cong \omega_0 LQ \tag{2.23}$$
$$Z_{BR}(\omega_0) = \sqrt{(1+Q^2)\frac{L}{C_{eq}}} \cong Q\sqrt{\frac{L}{C_{eq}}}$$

Characteristic values of the bridge are provided in Table 2-2.

Table 2-2 Voltage source and impedance at resonance of an exemplary sensing bridge with parameters from Table 2-1

Parameter	Description	Value
U_{BR}	Sensing bridge output voltage signal	23,88 mV
Z_{BR}	Sensing bridge source (output) impedance	527,8 kΩ

2.1.2 Bridge Voltage and Capacitance Measurement Noise

The detailed noise analysis in 2.8.4 will show that the dominant voltage noise of the sensing circuit is the thermal noise generated by the real (dissipative) part of bridge source impedance. The standard definition for the noise Amplitude Spectrum Density (ASD) of a resistor, expressed in $\mathrm{V}/\sqrt{\mathrm{Hz}}$, is

$$S_{u-BR-th}^{1/2}(\omega) = \sqrt{4k_B T\Re[Z_{BR}(\omega)]} \tag{2.24}$$

where $S_{u-BR-th}^{1/2}(\omega)$ is the thermal noise ASD of the sensing bridge, k_B is the Boltzmann constant $1{,}38 \cdot 10^{-23}$ $\mathrm{m^2kgs^{-2}/K}$ and T is the absolute temperature. At the resonance, the bridge impedance (2.23) is real and the bridge thermal noise can be written as

$$S_{u-BR-th}^{1/2}(\omega) = \sqrt{4k_B T\omega_0 L\frac{1+Q^2}{Q}} \cong \sqrt{4k_B T\omega_0 LQ} \tag{2.25}$$

To calculate the capacitance measurement noise, the bridge voltage noise must be converted into equivalent input referred capacitance noise by dividing the voltage noise with the conversion factor, i.e., the capacitance to voltage gain $|\partial U_{BR}/\partial\Delta C|$. From (2.18) and (2.23), the conversion factor at resonant frequency can be written as

$$\left|\frac{\partial U_{BR}}{\partial \Delta C}\right| = |j\omega Z_{BR}(\omega_0)\cdot U_M| = \omega_0|Z_{BR}(\omega_0)|U_M = \omega_0^2 LQU_M \tag{2.26}$$

The ASD of the equivalent input capacitance noise is calculated from (2.25) and (2.26).

$$S_{\Delta C-BR-th}^{1/2}(\omega) = \frac{S_{u-BR-th}^{1/2}(\omega)}{\left|\frac{\partial U_{BR}}{\partial \Delta C}\right|} = \frac{1}{U_M}\sqrt{\frac{4k_B T}{\omega_0^3 LQ}} \tag{2.27}$$

So far in the noise analysis, it is assumed that the bridge thermal noise is the dominant noise of the sensing circuit and that the gain of the following stages does not affect the noise level. However, the bridge output is an amplitude modulated signal with the carrier frequency ω_0 that shall be demodulated and this will change the noise density. It will be shown in 2.10 that the demodulation process will double the noise Power Spectral Density (PSD), or

$$S_{out}(\omega_{LF}) = 2S_{in}(\omega_0) \tag{2.28}$$

This requires a large separation of the frequencies, $\omega_{LF} << \omega_0$, where "LF" stands for a low frequency band of interest (f_{LF} < 1 Hz in LTP and LISA). The sensing bridge thermal noise has a more or less constant power spectrum in the band $\omega_{LF} \pm 1/\tau$, where τ is the effective time constant of the demodulation output low-pass filter. For such a noise source the demodulated output will be white in the band from DC to $1/\tau$.

It is clear from (2.28) that the ASD of the voltage and capacitance noise after demodulation is larger by factor $\sqrt{2}$ than before demodulation.

$$S_{u-BR-th}^{1/2}(\omega_{LF}) = \sqrt{2} \cdot S_{u-BR-th}^{1/2}(\omega_0) = \sqrt{8k_B T \omega_0 LQ} \tag{2.29}$$

$$S_{\Delta C-BR-th}^{1/2}(\omega_{LF}) = \sqrt{2} \cdot S_{\Delta C-BR-th}^{1/2}(\omega_0) = \frac{1}{U_M}\sqrt{\frac{8k_B T}{\omega_0^3 LQ}} \tag{2.30}$$

Important conclusions regarding capacitance measurement can be derived from (2.30):

- Noise in capacitance sensor is smaller when larger TM injection voltage U_M is used, i.e., the SNR improves with a higher injection level. As already stated, the injection level cannot be arbitrary because it would generate back-action force noise on the TM via electrostatic actuation
- As the bridge thermal noise is the dominating noise (and shown here as the only one) it would be favorable to reduce it by operating the sensing bridge at a very low temperature, which puts large constraints on the spacecraft thermal control design. It will be shown that the other bridge parameters can be selected in a way that makes it possible to lower capacitance noise enough to fulfill the top-level requirements
- The selection of the resonant frequency ω_0 is a dominant factor in noise reduction (ω_0^3), but there are also limits in the electronics and the transformer design that do not allow this frequency to be very high. The bridge circuit quality factor Q depends also on the *tan* δ of the insulating dielectric in external coaxial cables towards TM electrodes and the *tan* δ of the resonant tuning capacitors, which become worse at higher frequencies. Thus, the frequency increase will at some level start reducing the quality factor and amplify the noise
- Larger inductance of the transformer is beneficial, requiring larger ferrite cores, which then goes against achieving a high quality factor of the transformer. This analysis will be provided in 2.7.1

With the resonant frequency f_0 = 100 kHz, the operating temperature T = 300 K and the sensing bridge parameters from Table 2-1, the capacitance noise ASD of the simplified sensing circuit defined by (2.30) is $0{,}66 \times 10^{-18}\ \mathrm{F}/\sqrt{\mathrm{Hz}} = 0{,}66\ \mathrm{aF}/\sqrt{\mathrm{Hz}}$.

2.1.3 Position Measurement – TM Sensing Noise

The conversion from capacitance to position measurement noise refers to Figure 2-8.

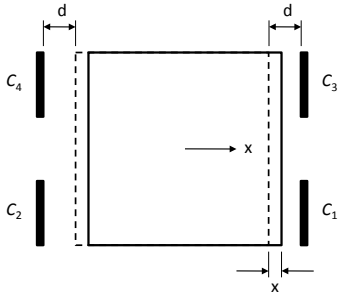

Figure 2-8 The TM with four sensing electrodes, which allows detection of its translational and rotational movement. In the centered position the gap between the TM and the electrodes is d = 4 mm in "x" sensing axis and nominal capacitance is ≈1,15 pF

The TM forms the air capacitances with electrodes defined as follows

$$C_0 = \varepsilon_0 \frac{A}{d} \tag{2.31}$$

$$C_1 = \varepsilon_0 \frac{A}{d-x} = C_0 \frac{1}{1-\frac{x}{d}} \tag{2.32}$$

$$C_2 = \varepsilon_0 \frac{A}{d+x} = C_0 \frac{1}{1+\frac{x}{d}} \tag{2.33}$$

where A is the electrode area, ε_0 is the permittivity of free space, d is the nominal TM – electrode gap for the centered TM and x is the TM displacement from center. The sensing bridge is connected between electrodes C_1 and C_2 (second channel between electrodes C_3 and C_4) and it measures the difference between two capacitances, which can be approximated with

$$\Delta C = C_1 - C_2 = 2C_0 \frac{x}{d}\left[1 - \left(\frac{x}{d}\right)^2\right]^{-1} \cong 2C_0 \frac{x}{d} \tag{2.34}$$

for the "performance" sensing range of $x \leq \pm 10$ μm from the centered position.

The position noise ASD, $S_x^{1/2}(\omega_{LF})$ in $\mathrm{m}/\sqrt{\mathrm{Hz}}$ is converted from the capacitance noise (2.30) by dividing the latter with the capacitance-to-position gradient $|\partial \Delta C/\partial x|$ that can be derived from (2.34) as

$$\left|\frac{\partial \Delta C}{\partial x}\right| = 2\frac{C_0}{d} \tag{2.35}$$

$$S_x^{1/2}(\omega_{LF}) = \frac{S_{\Delta C-BR-th}^{1/2}(\omega_{LF})}{\left|\frac{\partial \Delta C}{\partial x}\right|} = \frac{1}{U_M}\frac{d}{C_0}\sqrt{\frac{2k_B T}{\omega_0^3 LQ}} \tag{2.36}$$

In addition to the parameters analyzed in the discussion of the capacitance noise (2.30), it is evident from (2.36) that the reduction of the sensing gap d and the enlargement of area of electrodes A, i.e., the enlargement of capacitance C_0, would further reduce the sensing position noise. A larger electrode area would lead to a larger sensor, i.e., a larger TM and its enclosure. While a larger sensor is constrained only with technological limitations, the reduction of the gap introduces difficulties to model couplings with the TM, which decrease quickly with electrode-to-TM separation. These include TM charging and patch charge effects [24], which both produce couplings decreasing at $1/d^3$.

Sensing position noise does not need to be as low as possible, which is the goal of the accelerometer applications for the space missions. The LISA sensor will be designed to minimize the total stray forces (accelerations) on the TM [20], which can be achieved by arranging several parameters, not just by minimizing sensing noise.

Note that according to Figure 2-2, outputs of two sensing channels, each connected to a pair of electrodes, are added to calculate TM displacement. For equal displacement outputs, $x = x_1 = x_2$ and equal root mean square (RMS) noise, $x_n = x_{n1} = x_{n2}$, this scheme reduces the combined displacement noise x_{n-comb} by factor $\sqrt{2}$ and thus improves the SNR by the same factor.

$$\begin{aligned} x_{comb} &= \frac{x_1 + x_2}{2} = x \\ x_{n-comb} &= \frac{\sqrt{x_{n1}^2 + x_{n2}^2}}{2} = \frac{x_n}{\sqrt{2}} \\ SNR_{comb} &= \frac{x_{comb}}{x_{n-comb}} = \sqrt{2}\frac{x}{x_n} = \sqrt{2} \cdot SNR \end{aligned} \tag{2.37}$$

Hence, the position noise ASD of the single channel (2.36) is in the combined sensing output, $S_{x-comb}^{1/2}(\omega_{LF})$ scaled down with the same $\sqrt{2}$ factor

$$S_{x-comb}^{1/2}(\omega_{LF}) = \frac{1}{U_M}\frac{d}{C_0}\sqrt{\frac{k_B T}{\omega_0^3 LQ}} \tag{2.38}$$

With the resonant frequency f_0 = 100 kHz, the operating temperature T = 300 K, the nominal sensing gap d = 4 mm and the exemplary sensing bridge parameters from Table 2-1, the position noise ASD of the combined output is $0{,}82\ \mathrm{nm}/\sqrt{\mathrm{Hz}}$.

2.2 Back-Action Force and Acceleration Noise of the Readout Circuit

The discussion in this section will often refer to the spring stiffness coefficient $k = -\partial F/\partial x$ with the unit kg/s^2, describing the resistance to deformation by an applied force. Similarly, one can introduce the stiffness per unit mass or gravitational stiffness or simply stiffness $\omega^2 = -m^{-1}\,\partial F/\partial x$ with the unit s^{-2}, describing the resistance to deformation (displacement) by an applied acceleration (gravitation).

In LISA drag-free control, the position of the free-falling TM is measured by the readout (sensing circuit); this information is then used by the drag-free attitude control system (DFACS) to control the spacecraft (S/C) so that it follows the TM (Figure 2-9). The S/C is used to protect the TM by shielding it from external disturbing forces $F_{S/C}$. These forces acting on S/C are due to the striking particles coming from the sun (solar wind) and from outer space, but also include the S/C thrusters' noise (jitter) and the difference in the gravitational acceleration between the TM and the S/C center of mass.

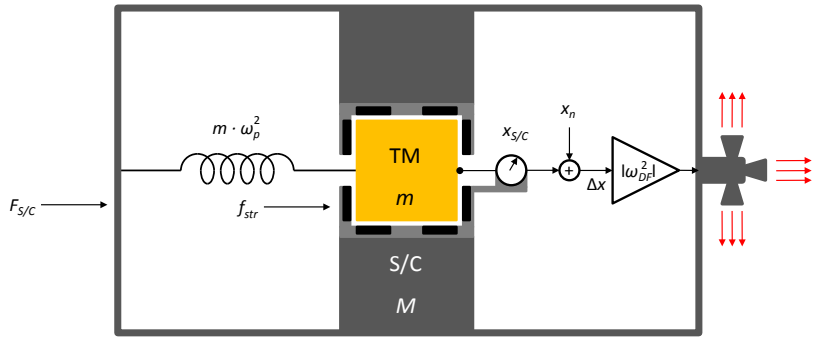

Figure 2-9 The TM (mass m), surrounded by sensing electrodes and protected by the S/C (mass M), is affected by a spring-like, position-dependent coupling ω_p between the TM and S/C and by position-independent internal stray forces f_{str}. The readout with position noise x_n measures the relative position of S/C against the TM, which the S/C drag-free controller is minimizing by actuating precision S/C thrusters to follow the free-falling TM and at the same time to counteract the external forces on S/C

Most of the TM to S/C position-independent stray forces f_{str} are of S/C origin, for instance, those due to thermal noise, pressure fluctuation etc. Also, the non-gravitational unshielded external forces, e.g., the cosmic rays that are not blocked by the S/C, are represented by these position-independent stray forces. The capacitive readout with its position noise x_n is driving the thrusters via the DFACS control gain $|\omega_{DF}^2|$ and thus producing the disturbing random forces. The position-dependent internal forces on the TM are produced by the residual S/C to TM motion that multiplies with the spring-like stiffness $k_p = m \cdot \omega_p^2$, i.e., a coupling with its origin in any DC force gradients summarized by ω_p, the natural frequency of the TM oscillation relative to the S/C.

At a high control loop gain $|\omega_{DF}^2|$ and in the absence of gravitation, the residual TM accelerations a_n [16] can be written as

$$a_n \cong \frac{f_{str}}{m} + \omega_p^2 \left(x_n + \frac{F_{S/C}}{M \omega_{DF}^2} \right) = \frac{f_{str}}{m} + \omega_p^2 \Delta x \tag{2.39}$$

where m is the TM mass, M is the S/C mass, and Δx is the residual jitter between the S/C and the TM. It has already been said that for LISA to be successful the TM residual acceleration must be minimized. Therefore, it does not help if only the readout sensing noise x_n is reduced. Instead, the product $\omega_p^2 \Delta x$ and the f_{str} must be reduced. While for the space accelerometers the S/C acceleration is minimized, the LISA goal is to minimize the part of the TM acceleration, which is not due to gravitational forces.

The residual parasitic stiffness ω_p^2 between the S/C and the TM cannot be completely eliminated due to the S/C self-gravity (in spite of mass balancing) and the sensor itself. Any voltage drop between the TM and the surrounding electrodes generates a position-dependent force $F(x)$ and thus a stiffness ω_p^2 proportional to the force gradient $\partial F / \partial x$. This stiffness is negative, i.e., it acts as a negative spring [25]. The effect is that the TM is unstable towards electrostatically attracting sensor walls, which requires compensation by the DFACS control loop in the form of electrostatic actuation along the non-drag-free axes, i.e., axes that are not in line with the laser interferometer.

According to Figure 2-8, the TM, its surrounding electrodes and other sensor walls (e.g., guard rings around electrodes at zero potential) constitute a multi-capacitor with stored potential electrostatic energy $= C_{tot} U_\Delta{}^2/2$, where the total capacitance $C_{tot} = \sum_j C_j$ is the sum of all capacitances that the TM makes with all sensor surfaces and U_Δ is the voltage drop

between the TM and these surrounding surfaces. The electrostatic force around the *x*-axis exerted on the TM by four electrodes is the position differential of the electrostatic potential written as

$$F_x = \frac{1}{2}\sum_{j=1}^{4}\frac{\partial C_j}{\partial x}\left(U_{TM} - U_j\right)^2 = \frac{1}{2}\sum_{j=1}^{4}\frac{\partial C_j}{\partial x}\langle U_{TM}^2\rangle \tag{2.40}$$

where the TM is biased with the sinusoidal AC voltage U_{TM} applied via injection electrodes and the electrodes are kept at zero potential (U_j=0) by the readout circuit. The latter is true because the sensing amplifiers will keep the transformer bridge secondary at the virtual ground, which will then also keep the electrodes connected to transformer primary windings at zero potential. With very low TM displacement bandwidth, only the DC component (the average) of the square of the TM voltage, i.e., $\langle U_{TM}^2\rangle$, will be responsible for the generated force.

From the definition of capacitances on each side of the TM (2.32) and (2.33), the first capacitance derivative (capacitance gradient) for small TM displacement *x* around the middle position (x = 0), can be easily calculated by

$$\frac{\partial C}{\partial x} = \frac{\partial}{\partial x}\left(C_0\frac{1}{1 \pm \frac{x}{d}}\right) = C_0\frac{\mp\frac{1}{d}}{\left(1 \pm \frac{x}{d}\right)^2} \xrightarrow{x\to 0} \mp\frac{C_0}{d} \tag{2.41}$$

The TM injection (bias) voltage is a sinusoidal signal with amplitude U_M and frequency f_0, nominally selected to be 100 kHz. The average of the square of the sinusoidal signal is equivalent to half of the squared peak amplitude of the signal as calculated below.

$$\langle U_{TM}^2\rangle = \langle U_M^2 \sin^2\omega_0 t\rangle = \langle\frac{U_M^2}{2}(1 - \cos 2\omega_0 t)\rangle = \frac{U_M^2}{2} \tag{2.42}$$

The presence of the injection voltage U_{TM} on the TM generates stiffness, i.e., coupling between the readout circuit and the TM, because any voltage noise on electrodes like U_j in (2.40) will interact with U_{TM} and generate force, called readout back-action force. Gravitational stiffness, as has already been mentioned, is proportional to the force gradient and can be written by use of (2.40) and (2.42) as

$$\omega_p^2 = -\frac{1}{m}\frac{\partial F}{\partial x} = -\frac{1}{2m}\frac{U_M^2}{2}\sum_{j=1}^{4}\frac{\partial^2 C_j}{\partial x^2} \tag{2.43}$$

The second capacitance derivative can be easily calculated from (2.41) and written as

$$\frac{\partial^2 C}{\partial x^2} = \frac{\partial}{\partial x}\left(\frac{\partial C}{\partial x}\right) = \frac{\partial}{\partial x}\left[C_0\frac{\mp\frac{1}{d}}{\left(1 \pm \frac{x}{d}\right)^2}\right] = C_0\frac{2\left(\pm\frac{1}{d}\right)^2}{\left(1 \pm \frac{x}{d}\right)^3} \xrightarrow{x\to 0} \frac{2C_0}{d^2} \tag{2.44}$$

which summed over four electrodes is

$$\sum_{j=1}^{4}\frac{\partial^2 C_j}{\partial x^2} = \frac{8C_0}{d^2} \tag{2.45}$$

By substituting (2.45) into (2.43), the readout stiffness produced by all four electrodes of one sensing axis can be written as

$$\omega_p^2 = -2\frac{C_0}{m}\left(\frac{U_M}{d}\right)^2 = -2\varepsilon_0\frac{A}{m}\frac{U_M^2}{d^3} \tag{2.46}$$

It is important to note the following:

- Since the stiffness is proportional to the square of injection voltage U_M, the voltage reduction will effectively reduce the stiffness and thus the back-action force, but will also reduce the readout sensitivity. To be compliant with the top level stray acceleration requirements, a compromise has been found prior to this dissertation by selecting a TM injection amplitude level of 0,6 V (0,42 V_{RMS})
- The reduction of the stiffness level by enlargement of the sensing gap d is very effective since it is proportional to the cube of the gap (2.46). In addition, the electrode to TM couplings that become dominant with small gaps quickly diminish with larger gaps. Since these couplings are difficult to model, larger gaps will ensure more accurate performance estimation. This has influenced the decision to select mm size gaps between the TM and the electrodes: 4 mm in *x*-axis, 2,9 mm in *y*-axis and 3,5 mm in *z*-axis

The spring-like stiffness generated by both sensing channels on one measurement axis can be simply calculated as

$$k_p = m \cdot \omega_p^2 = -2C_0\left(\frac{U_M}{d}\right)^2 = -2\varepsilon_0 A\frac{U_M^2}{d^3} \tag{2.47}$$

This stiffness generates readout back-action force on the TM proportional to the TM displacement from the center that can be written as

$$F_{ba\_x} = |k_p| \cdot x = 2C_0\left(\frac{U_M}{d}\right)^2 x \tag{2.48}$$

from which one can deduce that the ASD of force and of displacement noise are similarly related. This allows calculating the TM back-action force noise from (2.47) and (2.38)

$$S_{F_{ba}}^{1/2} = |k_p| \cdot S_{x-comb}^{1/2} = 2\frac{U_M}{d}\sqrt{\frac{k_B T}{\omega_0^3 LQ}} \tag{2.49}$$

and the back-action acceleration noise arising from the sensing bridge thermal (dominating) noise and TM injection voltage needed to operate the sensing readout.

$$S_{a_{ba}}^{1/2} = \frac{1}{m} \cdot S_{F_{ba}}^{1/2} = |\omega_p^2| \cdot S_{x-comb}^{1/2} = \frac{2}{m}\frac{U_M}{d}\sqrt{\frac{k_B T}{\omega_0^3 LQ}} \tag{2.50}$$

The parameters of an exemplary sensor are given in Table 2-3. “Sensor” refers to the TM surrounded by the electrodes and the sensing readout circuit. The corresponding back-action stray force and acceleration as well as couplings between the readout electronics, i.e., between the S/C (note that electronics are mounted on S/C) and the TM, are calculated in Table 2-4.

Table 2-3 Parameters of an exemplary gravitational sensor

Parameter	Description	Value
U_M	TM peak injection voltage (100 kHz)	0,6 V
ω_0	Injection voltage natural frequency ($2\pi \cdot 100$ kHz)	628319 s^{-1}
C_0	Nominal capacitance in x-axis for a centered TM	1,15 pF
d	Sensing gap in x-axis	4 mm
m	TM mass	1,96 kg
k_B	Boltzmann constant	$1{,}38 \cdot 10^{-23}\ \frac{m^2 kg}{s^2 K}$
T	Absolute temperature	300 K
L	Transformer winding inductance	4,2 mH
Q	Sensing bridge (transformer) quality factor	200

Table 2-4 The sensing readout coupling to the TM and resulting back-action for sensor parameters defined in Table 2-3

Parameter	Description	Value
$\lvert\omega_p^2\rvert$	Stiffness per unit mass arising from the readout noise	$0{,}26 \cdot 10^{-7}\ s^{-2}$
$\lvert k_p\rvert$	Spring-like stiffness, $m \cdot \lvert\omega_p^2\rvert$	$0{,}52 \cdot 10^{-7}\ \frac{N}{m}$
$S_{F_{ba}}^{1/2}$	Sensing readout back-action force on the TM	$0{,}042\ \frac{fN}{\sqrt{Hz}}$
$S_{a_{ba}}^{1/2}$	Sensing readout back-action acceleration on the TM	$0{,}022\ \frac{fm}{s^2\sqrt{Hz}}$

2.3 Main Sensing Requirements

Top science requirements, from which the TM sensing requirements can be derived, have their origin in the residual TM stray acceleration defined by the (2.39). The LISA and the LPF (LTP) mission requirements [9] and [26] set the target gravitational sensitivities in terms of maximum stray acceleration. The maximum stray acceleration in LISA is

$$S_a^{1/2} \leq 3\left[1+\left(\frac{f}{3\ \text{mHz}}\right)^2\right]\frac{\text{fm}}{\text{s}^2\sqrt{\text{Hz}}} \tag{2.51}$$

in the LISA bandwidth 0,1 mHz $\leq f \leq$ 0,1 Hz

In LTP, the requirement is relaxed 10 times in terms of acceleration level and frequency

$$S_a^{1/2} \leq 30\left[1+\left(\frac{f}{3\ \text{mHz}}\right)^2\right]\frac{\text{fm}}{\text{s}^2\sqrt{\text{Hz}}} \tag{2.52}$$

in the LTP bandwidth 1 mHz $\leq f \leq$ 30 mHz

These two requirements are shown in Figure 2-10.

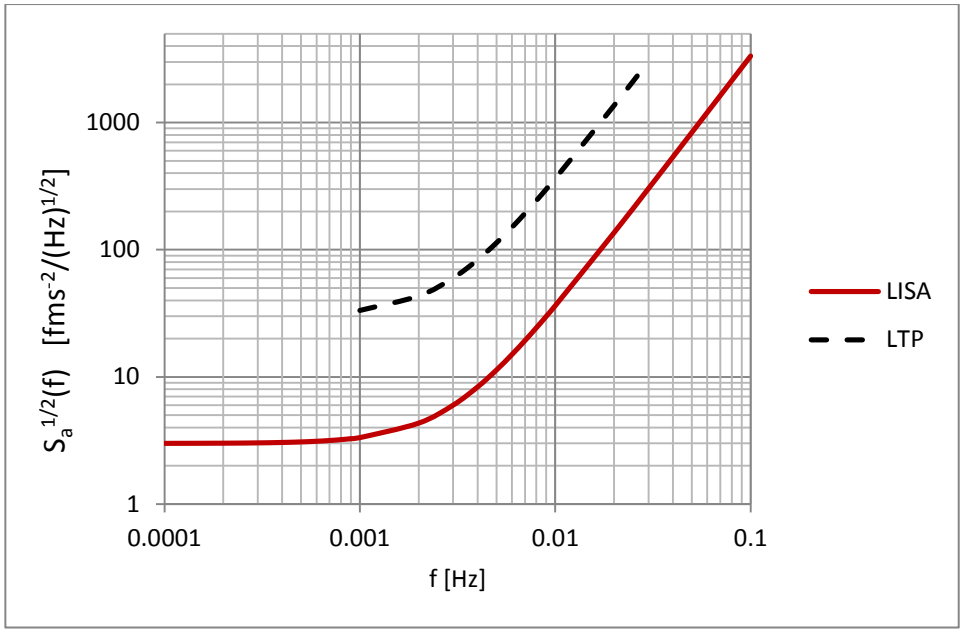

Figure 2-10 Maximum stray acceleration limits for LISA and LTP and their bandwidths

The f^2 noise amplification in acceleration ASD above 3 mHz is expected to be constrained by the nearly quantum-limited displacement sensitivity of the laser interferometer. The detection of the gravitational waves is proportional to the position sensitivity of the laser interferometer, i.e., the ability to detect small modulations of distance between two free-falling TMs. The position noise is converted from force or acceleration noise (2.39) by factor $1/\omega^2$ and since the electronics noise is growing at low frequencies, the detection of the displacements at very low frequencies is difficult. Hence, the detection of the gravitational strain in LISA is decaying by factor $1/f^2$ below 100 μHz, as shown in Figure 2-11.

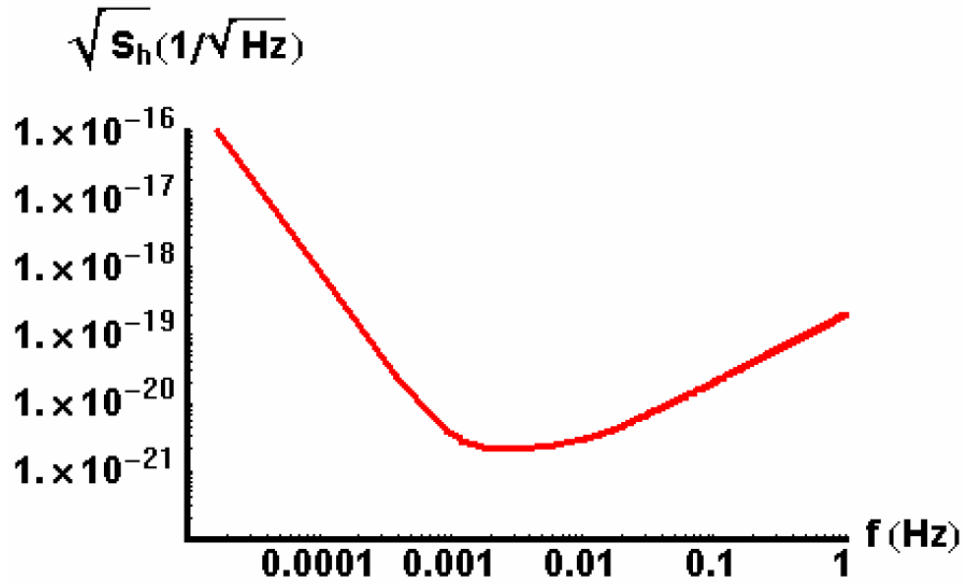

Figure 2-11 LISA gravitational strain sensitivity curve, i.e., the ability to detect relative arm length variation between two TMs, $S_h{}^{1/2}$ in $1/\sqrt{Hz}$

The flow down of the top-level acceleration requirements to the sensing specific requirements is discussed and analyzed in the following paragraphs.

The dominant stray acceleration noise in the total $3\ \mathrm{fms^{-2}/\sqrt{Hz}}$ LISA acceleration budget comes from the TM actuation noise. The readout (sensing) back-action contribution is limited to 1/10th of the total limit to provide a safe margin [26].

$$S_{a_{ba}}^{1/2} \leq 0{,}3\left[1+\left(\frac{f}{3\ \mathrm{mHz}}\right)^2\right]\frac{\mathrm{fm}}{\mathrm{s^2\sqrt{Hz}}} \tag{2.53}$$

The sensor position noise and stiffness related to the readout AC injection bias voltage on TM, x_n and ω_p^2 in (2.39) are limited in [26] to

$$S_{x_n}^{1/2} \leq 1{,}8\left[1+\left(\frac{f}{3\ \mathrm{mHz}}\right)^2\right]\frac{\mathrm{nm}}{\sqrt{\mathrm{Hz}}} \tag{2.54}$$

$$\left|\omega_p^2\right| \leq 0{,}5\cdot 10^{-7}\frac{1}{\mathrm{s^2}} \tag{2.55}$$

The position noise limit (2.54) is given for two combined sensing channels from which displacement and rotation are calculated. This means that each channel could have a larger noise limit by factor $\sqrt{2}$. To include an additional margin, the sensing design will not consider this relaxation factor. The injection voltage-related stiffness limit (2.55) represents a very small part of the total maximum stiffness of $13{,}5\cdot 10^{-7}\mathrm{s^{-2}}$ [26].

The main parameters of the gravitational sensor core, i.e., the mass (*m*) of the TM, size (area *A*) and gaps (*d*) of surrounding electrodes are derived from the stiffness requirement and the requirement for the level of the injection voltage U_M. The final TM geometry is given in Table 2-5 and [25]. With other parameters given in Table 2-3, the stiffness, position and back-action acceleration noise requirements, shown in Table 2-6, are satisfied on all axes.

Table 2-5 The sensor geometry

Axis	Single electrode area *A*	Electrode gap *d*	Nominal capacitance C_0
x	1,45 x 3,60 = 5,220 cm^2	4,0 mm	1,1555 pF
y	0,71 x 3,82 = 2,712 cm^2	2,9 mm	0,8281 pF
z	0,65 x 3,70 = 2,405 cm^2	3,5 mm	0,6084 pF

Table 2-6 The stiffness and sensing noise ASD for sensor parameters given in Table 2-3

Axis	$\left\|\omega_p^2\right\|$	$S_{x_n}^{1/2}$	$S_{a_{ba}}^{1/2}$
x	$0{,}265\cdot 10^{-7}\ \mathrm{s^{-2}}$	$0{,}813\ \frac{\mathrm{nm}}{\sqrt{\mathrm{Hz}}}$	$0{,}022\ \frac{\mathrm{fm}}{\mathrm{s^2\sqrt{Hz}}}$
y	$0{,}362\cdot 10^{-7}\ \mathrm{s^{-2}}$	$0{,}823\ \frac{\mathrm{nm}}{\sqrt{\mathrm{Hz}}}$	$0{,}030\ \frac{\mathrm{fm}}{\mathrm{s^2\sqrt{Hz}}}$
z	$0{,}182\cdot 10^{-7}\ \mathrm{s^{-2}}$	$1{,}352\ \frac{\mathrm{nm}}{\sqrt{\mathrm{Hz}}}$	$0{,}025\ \frac{\mathrm{fm}}{\mathrm{s^2\sqrt{Hz}}}$

The stiffness, position noise and the sensor back-action acceleration are calculated by (2.46), (2.38) and (2.50), respectively.

Note that the stiffness depends only on the sensor geometry and the injection voltage amplitude U_M. The largest sensing noise appears on the *z*-axis due to the smallest electrode area, i.e., the sensing capacitance C_0. The *y* and *z* electrodes are smaller compared to the *x* electrodes, (Figure 2-1), to provide space for the injection electrodes [25]. The sensing back-action acceleration $S_{a_{ba}}^{1/2}$ is 10 times smaller than the limit given by (2.53) and thus it is negligible. Note that this performance assumes the sensing transformer design to be with *L* =

4,2 mH and Q = 200. The transformer design requiring large inductance and a large quality factor at 100 kHz is very challenging.

2.3.1 Sensing Range, Noise and TM Injection Voltage Stability

The sensing circuit is a capacitance meter and thus it is more reasonable to define the sensing requirements in terms of capacitance rather than TM position. In addition, the relationship between the sensing output and the input capacitance is linear. The sensing circuit noise, Table 2-7, expressed as the input capacitance noise, is equal for all three axes. On the other hand, if expressed as the input position noise, it can be larger for the *z*-axis because of small *z* electrodes.

Table 2-7 The sensing noise requirements

Axis	Capacitance-to-position gradient $\left\lvert\frac{\partial \Delta C}{\partial x}\right\rvert$	Capacitance noise requirement	Position noise requirement
x	$577{,}75\ \frac{\mathrm{pF}}{\mathrm{m}}$	$1\ \frac{\mathrm{aF}}{\sqrt{\mathrm{Hz}}}$	$1{,}731\ \frac{\mathrm{nm}}{\sqrt{\mathrm{Hz}}}$
y	$571{,}10\ \frac{\mathrm{pF}}{\mathrm{m}}$	$1\ \frac{\mathrm{aF}}{\sqrt{\mathrm{Hz}}}$	$1{,}751\ \frac{\mathrm{nm}}{\sqrt{\mathrm{Hz}}}$
z	$347{,}66\ \frac{\mathrm{pF}}{\mathrm{m}}$	$1\ \frac{\mathrm{aF}}{\sqrt{\mathrm{Hz}}}$	$2{,}876\ \frac{\mathrm{nm}}{\sqrt{\mathrm{Hz}}}$

The differential capacitance-to-position gradient is calculated by (2.35). The position noise is calculated by dividing the capacitance noise by the gradient as in (2.36).

The full range of the High Resolution (HR) mode, also called the Science Mode range, is ±200 μm [23]. This is the range in which the TM is found following the unlocking and the initial stabilization by the electrostatic actuation. The sensing noise requirements are not constant in the HR range. The sensing range with the most stringent noise level, as per Table 2-7, is called the Performance Range of the HR mode. It is only ±10 μm [23] from the centered TM position because, in nominal operation, the DFACS control loop keeps the S/C centered with respect to the TM.

Since the sensing gaps are several millimeters, it is possible for the TM to be found outside the full HR range after release, for which the sensing function must extend throughout the whole gap size. Therefore, the Wide Range (WR) mode, also called the Non-Science Mode, is required to provide several millimeters of sensing range, depending on sensing sensitivity (electrode size and gap) of each axis.

The millimeter size sensing dynamic range with a very low sensing noise floor on a nanometer scale is the basis for the resolution requirement of the Analog-to-Digital (A/D) Converter (ADC), i.e., the 24-bit resolution according to the analysis in 2.11.

Since the 24-bit space-qualified ADC does not currently exist, only the 16-bit ADC can be used. To maintain the high resolution of sensing output with the lower resolution ADC, the sensing circuit must operate with two different analog gains and two corresponding operational modes (see 2.8.5). The HR mode has a higher gain and a lower range, while the WR mode has a lower gain and a larger range.

It has been already stated that the noise requirement cannot be equal in the whole sensing range. The reason for this is the amplitude stability of the TM AC injection voltage, which will be further analyzed in the text.

To overcome the need to specify different position sensing requirements for each axis (either displacement or rotation), the range requirements will be converted to capacitance and made

equal for all axes (channels), i.e., ±5,8 fF for the performance range, ±0,12 pF for the full range of the HR mode and ±2,5 pF for the range of the WR mode. Table 2-8 shows the relationship between the capacitance and the displacement range requirements according to (2.34).

Table 2-8 The sensing range requirements

Axis	Performance Range ±5,8 fF	HR Mode ±0,12 pF	WR Mode ±2,5 pF
x	±10,04 µm	±207,3 µm	±2,558 mm
y	±10,16 µm	±209,1 µm	±2,095 mm
z	±28,77 µm	±342,0 µm	±2,750 mm

The sensing noise limit for the performance range given in Table 2-7 is assumed to be constant in the whole performance range.

One should note from (2.18) that the TM excitation level, i.e., the injection voltage amplitude U_M, acts as a gain of the sensing circuit and that the $1\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ limit is selected for the 0,6 V TM excitation (2.30). Hence, it is easy to deduce that any fluctuation of this voltage multiplies with the actual TM position and mimics a noisy TM movement. The TM injection stability limit of $S^{1/2}_{\partial U/U_M} = 50\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ is selected in such a way [23] that when multiplied with the 10 µm performance range, or its capacitance equivalent of 5,8 fF, it generates about 30% of the sensing noise limit at the end of the performance range, i.e., $0{,}5\,\mathrm{nm}/\sqrt{\mathrm{Hz}}$ or $0{,}3\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$.

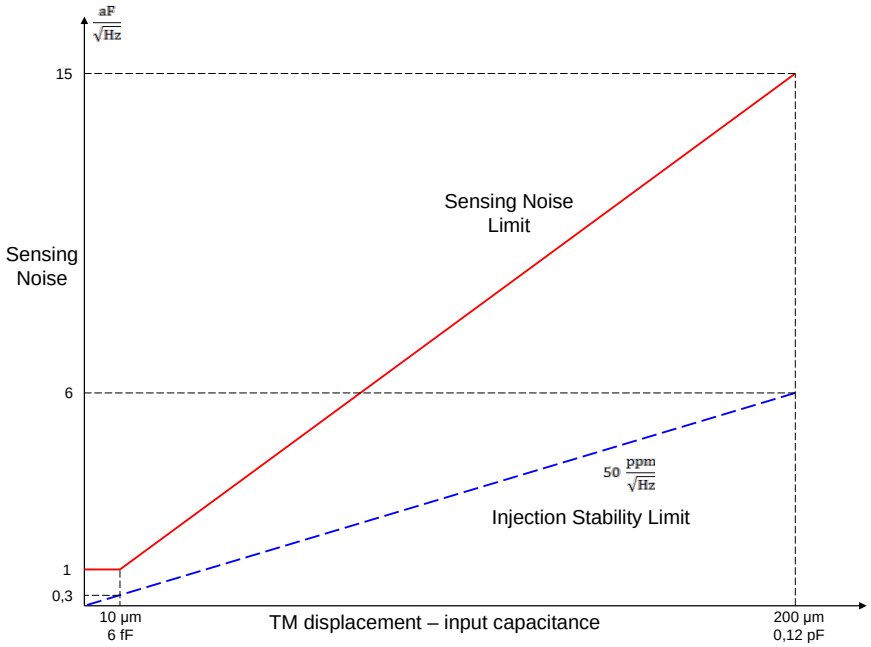

Figure 2-12 Sensing noise limit for the HR mode. At the end of the range, the TM excitation voltage fluctuation generates equivalent sensing noise of 40% of the total sensing noise limit

Beyond the performance range, the sensing noise limit must be relaxed due to injection stability, as shown in Figure 2-12, to the level of $15\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ at the end of the HR mode range. Similarly, the sensing noise limit in the WR mode is defined as shown in Figure 2-13.

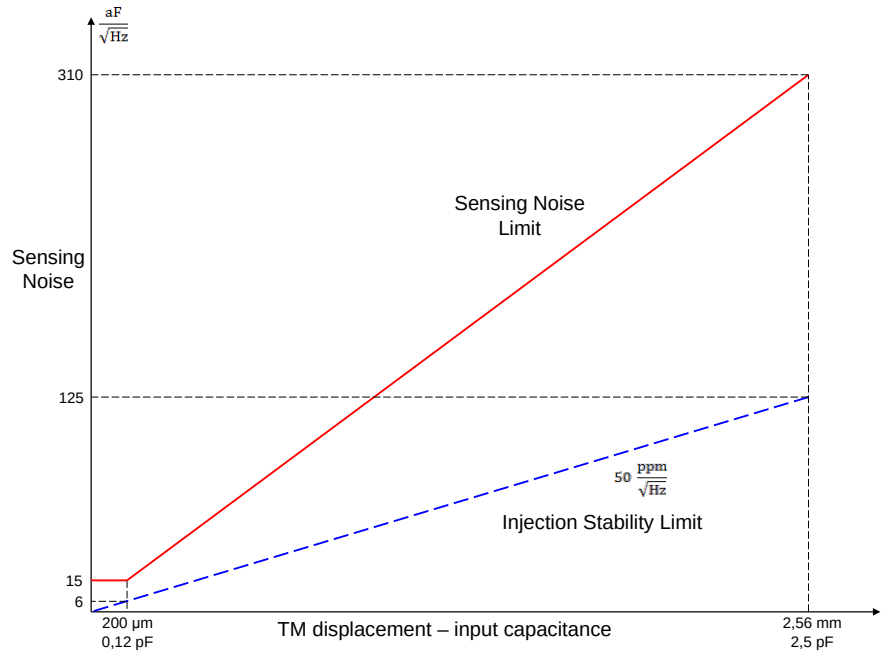

Figure 2-13 Sensing noise limit for the WR mode. The sensing noise limit is constant only in the small range of 200 µm, for which the injection voltage instability produces negligible noise

As expected, the design challenge will be to achieve the $1\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ noise level of the HR mode, in particular at the end of the performance range, i.e., at 5,8 fF differential capacitance.

2.3.2 Sensing Offset

The DFACS control loop is forcing the S/C to null the relative positional error between the S/C and the TM around all axes. The knowledge of the TM position in the performance range must be fairly accurate to prevent wrong positioning of the S/C and thus the misalignment of the laser beam with the center of the TM. The sensing offset will therefore be the knowledge uncertainty of the TM absolute position.

Despite the ability of the DFACS loop to maintain the residual error at a submicron level, the nominal operating (performance) range is set quite large, i.e., roughly 10 µm or 6 fF. This is because the location of the laser beam cannot be mechanically controlled very accurately and will be finally determined by measurement after the alignment of the laser optics. It is expected that the alignment will fall into the ±10 µm range with respect to the mechanical center of the TM electrode housing.

The sensing offset shall then be set to 10% of the range, i.e., ±1 µm or roughly ±600 aF when expressed in capacitance [23].

The sensing offset, also called position bias, has its source in the input and output stages of the sensing circuit. The simple electronics DC voltage offset at the end of the sensing chain is the first obvious cause. The offset in the sensing differential bridge (front-end stage) can cause a much larger offset and is more difficult to handle.

Any asymmetry or imbalance of the various parameters of the sensing bridge could easily dominate the whole offset budget. Since the front-end stage is operating in the AC mode, these asymmetries are demodulated in the last stage of the sensing circuit into the DC offset. This offset can be much larger than the DC offset voltage of the operational amplifiers of the last stage. Nevertheless, proper selection of the DC stage after the demodulator is also

important. In addition, the low frequency fluctuation of the offset must be small because it appears as a low frequency sensing noise.

The model of the sensing bridge addressing the sensing offset is derived in APPENDIX A.

From this model, represented by (A-16), one can derive three offset cases:

$$x_{BR0\_K} = \frac{d}{2}\left[(K_1 - K_2)\frac{C_a}{C_a + C_p}\right] \tag{2.56}$$

Offset x_{BR0_K} due to the transformer coupling $K_{1,2}$ asymmetry, in which the actuation filter capacitors $C_a = C_{a1} = C_{a2}$, the bridge resonance tuning capacitors $C_p = C_{p1} = C_{p2}$ and the transformer inductance imbalance $\Delta L = 0$.

$$x_{BR0\_C} = \frac{d}{2}\left(\frac{C_{a1}}{C_{a1} + C_{p1}} - \frac{C_{a2}}{C_{a2} + C_{p2}}\right) \tag{2.57}$$

Offset x_{BR0_C} due to the asymmetry of bridge capacitors C_a and C_p, in which $K_1 = K_2 = 1$ and $\Delta L = 0$.

$$x_{BR0\_L} = \frac{d}{4}\frac{\Delta L}{L}\frac{C_a}{C_a + C_p} \tag{2.58}$$

Offset x_{BR0_L} due to transformer inductance asymmetry, in which $C_a = C_{a1} = C_{a2}$, $C_p = C_{p1} = C_{p2}$ and $K_1 = K_2 = 1$.

All three offset cases (C_a and C_p separately) are illustrated in Figure 2-14.

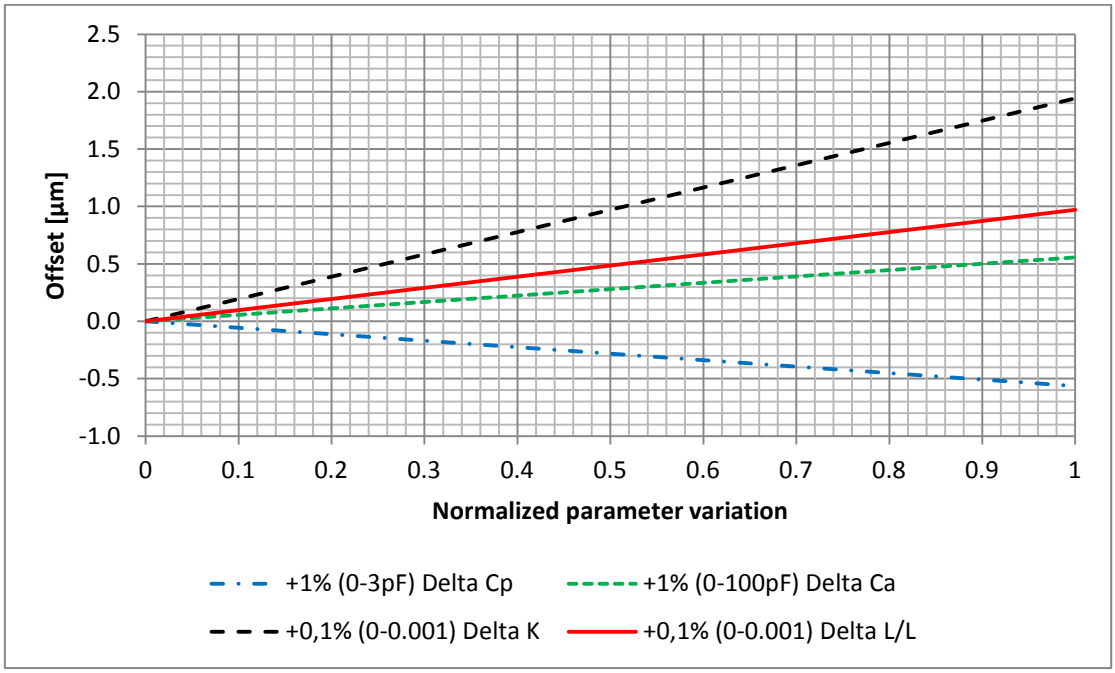

Figure 2-14 Sensing offset for the x-axis (electrode gap d = 4mm) due to asymmetry of bridge parameters: C_a, C_p of 1% and K, L of 0,1%

The transformer coupling K has the largest impact on the sensing offset, which generates twice the sensing offset limit of 1 µm with only 0,1% asymmetry. The transformer inductance L also has large impact. Relative asymmetry of 0,1% on L is equivalent to the offset limit. 1% of the tuning capacitance C_p, i.e., only 3 pF, generates an offset equal to half of the limit. Note that the same ±3 pF variation of tuning capacitance causes the shift from the best tuning frequency of ±0,5 kHz, which is considered the maximum acceptable

variation for which the sensing noise contribution of the front-end operational amplifiers is relatively low (Figure 2-31). Even though the variation in percentage of the actuation capacitor C_a has the same impact as the variation of C_p, the C_a variation is not restricted by the sensing noise level and thus, possible offset tuning can be easily made with 100 pF (1%) in case of C_a than with the 3 pF (1%) in case of C_p. The summary of the influence of the sensing bridge parameters is provided in Table 2-9.

Table 2-9 The variation of sensing bridge parameters for equivalent 1 µm sensing offset

Severity of influence	Parameter	Approximate nominal value	Relative variation for 1 µm offset	Equivalent absolute variation
1	K	1	515 ppm	0,000515
2	L	4 mH	1030 ppm	4,12 µH
3	C_p	300 pF	-17700 ppm	-5,31 pF
4	C_a	10 nF	18000 ppm	180 pF

Only the transformer relative inductance asymmetry $\Delta L/L$ was analyzed in the previous work and was limited in early FEE development to 100 ppm [25]. This was later reduced to 50 ppm [23], but only as a guideline to achieve the total sensing offset requirement. The 50 ppm value is, according to (2.58) and Table 2-9, equivalent to the position sensing offset of roughly 50 nm, i.e., 20 times below the offset limit of 1 µm, a really negligible contribution, but very challenging to achieve.

2.4 Sensing Channel Architecture

The architecture of one sensing channel (6 in total for each TM) is suggested in Figure 2-15, which follows the conceptual design shown in Figure 2-2.

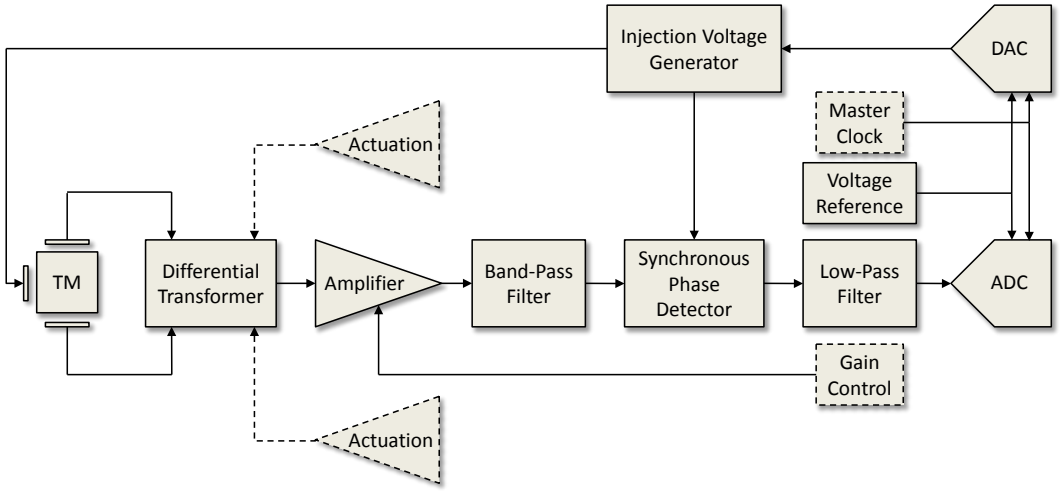

Figure 2-15 Architectural block diagram of one sensing channel connected to two electrodes

An AC signal in the form of a sinusoidal waveform is injected into the TM using injection electrodes. The amplitude of this waveform is controlled by the DAC and the stable voltage reference. The waveform frequency is derived from the master clock and fixed by digital control logic. The movement of the TM between the electrodes generates an amplitude modulated signal at injection (carrier) frequency with amplitude proportional to the level of the injection signal and the position of the TM between electrodes. This signal is amplified, band-pass filtered and only the frequency component in phase with the injection frequency is extracted using the lock-in technique consisting of the synchronous demodulation via phase

detection. The band-pass filtering is used to reduce the out-of-interest frequency spectral content that might leak through the non-ideal demodulator / detector. As the synchronous detection produces a DC signal of interest and the signal at twice the injection (carrier) frequency, the demodulator signal is low-pass filtered and the remaining DC signal is converted to a digital form by an ADC. The ADC compares the input signal with the stable voltage reference and samples it with the appropriate frequency, finally resulting in the required output data rate. In case the ADC resolution is not adequate for the whole sensing range of 2,5 mm (WR mode), a higher analog gain is applied for the 200 µm range (HR mode) to improve the resolution.

Note that the injection generator is common for all sensing channels. The detailed design and analysis of each of the sensing circuits are presented in the following sections.

2.5 Voltage Reference

It is evident from Figure 2-15 that the voltage reference could affect the performance of the TM injection voltage generator via the DAC and the sensing noise performance via the ADC. In addition, the voltage reference affects the actuation circuit, which will be analyzed in Chapter 3. Therefore, the voltage reference should be designed at least to fulfill the injection voltage and the sensing noise requirements.

2.5.1 Design requirement due to TM Injection Voltage Stability

According to the analysis in 2.3.1, the requirement for the amplitude stability of the TM excitation AC voltage is set to $S_{\partial U/U_M}^{1/2} = 50\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$. Note that this limit is approximately three times lower than the upper-level sensing requirement and thus provides some margin (Figure 2-12). Since the voltage reference is used to define the level of the AC amplitude (DAC), the same requirement applies to the relative amplitude stability of the voltage reference, i.e., $S_{\partial U/U_R}^{1/2} = 50\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$. For U_R = 10 V the voltage reference noise should be less than $500\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ in the LISA bandwidth of 0,1 mHz. Since the low frequency noise is dominated by the pink (flicker) noise with 1/f noise power density, the above requirement is actually the requirement for the maximum level of the 1/f noise at the lowest frequency of interest.

2.5.2 Design requirement due to Sensing Noise Limit

The ADC output is proportional to the ratio between the input voltage and the voltage reference. Accordingly, the intrinsic voltage reference noise is fully visible at the ADC output only when the input signal is at the full scale. The sensing capacitance noise floor limit is discussed in 2.3.1 and set to $S_C^{1/2} = 1\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ or the equivalent TM position noise of $S_{x_n}^{1/2} = 1{,}73\,\mathrm{nm}/\sqrt{\mathrm{Hz}}$ on the *x*-axis (Table 2-7). According to Figure 2-12, this noise limit is set for the ±6 fF performance range and is 15 times smaller than in the full measurement range of ±0,12 pF.

If the voltage reference level $\pm U_R$ is selected to equal the full scale capacitance input of ±0,12 pF, the required full scale noise limit of $15\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ (Figure 2-12) will be equivalent to the $125\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ noise, relative to the ADC full scale U_R. To provide a comfortable margin, the voltage reference noise can be set to $S_{\partial U/U_R}^{1/2} = 30\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$. Due to the ADC output voltage scaling, the reference noise is reduced 20 times in the ±6 fF performance range, i.e., to $0{,}18\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ or $1{,}5\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$. The required $1\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ noise limit for this reduced input range is equivalent to $8{,}33\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$, relative to the full scale of 0,12 pF. The $1{,}5\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ stability is thus considerably below this limit.

2.5.3 Expected Performance

The suitable voltage reference that can satisfy the requirements of 2.5.1 and 2.5.2 is the precision reference LT1021 from Linear Technology [27]. It is available in various voltages up to 10V and has a long space heritage. From the noise density graph, shown in [27] only down to 10 Hz, one can extrapolate the 1/f noise, convert it to the relative noise density expressed by (2.59) and plot it in Figure 2-16 against the requirements.

$$S_{\partial U/U_R}^{1/2} = 0{,}0125\,\frac{\text{ppm}}{\sqrt{\text{Hz}}} + \frac{0{,}04\ \text{ppm}}{\sqrt{f}} \tag{2.59}$$

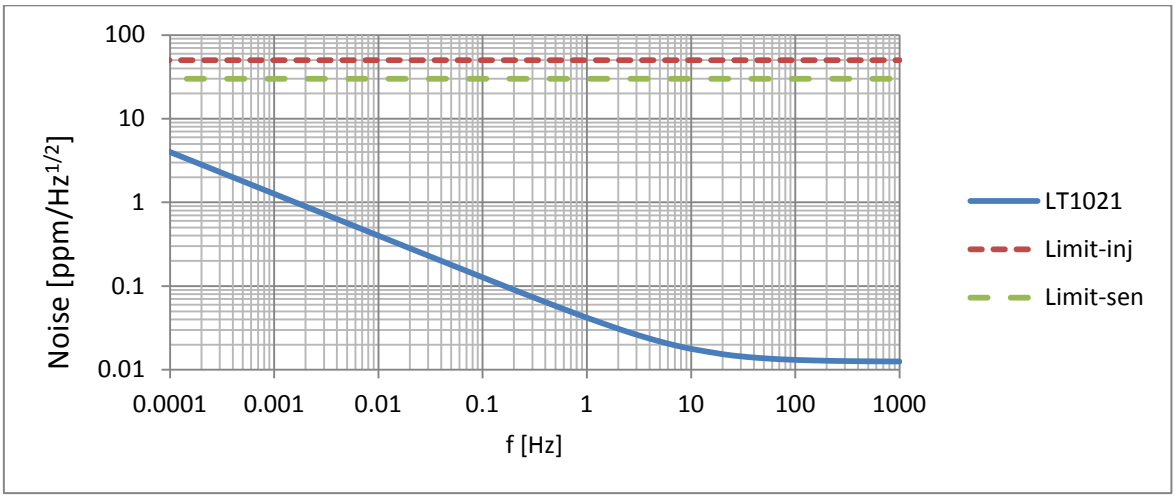

Figure 2-16 LT1021 voltage reference noise performance against the injection voltage stability and sensing noise design requirements. Even at 0,1 mHz, the margin is substantial

2.6 Injection Voltage Generator

The 100 kHz sinusoidal injection voltage (U_{INJ}) is electrostatically coupled to the TM excitation voltage (U_M) via six injection electrodes, Figure 2-17. Due to the stray capacitance of TM to the grounded electrode housing and twelve sensing electrodes with their own capacitances, the applied injection voltage is attenuated on the TM via the capacitance divider consisting of the aforementioned capacitances.

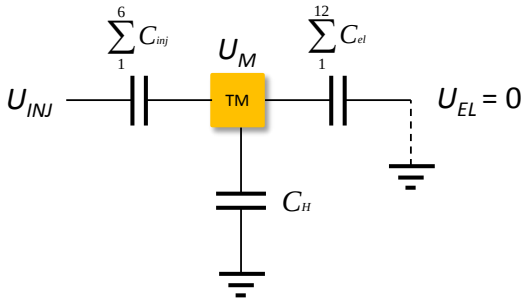

Figure 2-17 The injection capacitive divider made of 6 injection electrodes C_{inj}, 12 sensing electrodes C_{el} and a TM to electrode housing stray capacitance C_H. Electrode housing is grounded and electrodes are at zero potential via the sensing bridge

With the largest capacitance being the TM stray capacitance to ground C_H, the attenuation is according to (2.60) roughly 0,123, which requires about 4,8 V peak injection voltage to achieve the TM peak voltage of 0,6 V.

$$\frac{U_M}{U_{INJ}} = \frac{\sum_1^6 C_{inj}}{\sum_1^6 C_{inj} + \sum_1^{12} C_{el} + C_H} \cong 0{,}123 \tag{2.60}$$

It must not be forgotten that the U_M directly sets the sensitivity (gain) of the sensing circuit. In case the sensitivity of the sensor drops during the mission, it is useful to allow a possibility to vary injection voltage via the DAC. This does not necessarily have to be with high accuracy (low resolution DAC), but rather with high stability (voltage reference), as discussed in 2.5.1.

2.6.1 Possible Design Solutions

The initial development of the 100 kHz oscillator and the sinusoidal waveform generator is described in [16]. The first approach was based on 100 kHz quartz crystal with the servo control loop for amplitude stability. The second approach, with the block diagram shown in Figure 2-18, included the 10 MHz oscillator, a frequency divider to generate the square waveform of 100 kHz and a low-pass filter of 8th order to remove higher harmonics of the sinusoidal waveform. Both circuits showed large noise due to inadequate amplitude stability of about $1000\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ at 0,1 mHz ($50\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ required). One will note that in the second design the filtering is sharp, i.e., at 8th order, to attenuate the second harmonic already at 300 kHz.

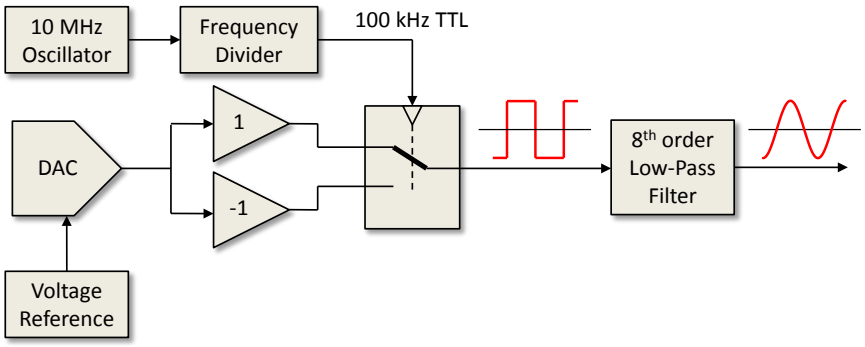

Figure 2-18 TM injection signal generated from 100 kHz pulsed waveform using high order low-pass filtering to remove 100 kHz harmonics

The direct digital syndissertation of the sinusoidal waveform, using, e.g., a waveform tick (sample) frequency of several MHz and consequently simpler low-pass filtering, would place the burden on the DAC selection, which would need to have a small settling time and would thus consume considerably more power. Due to drawbacks of the previous designs the following solution, shown in Figure 2-19, is suggested.

Much like in Figure 2-18, the amplitude is set by the DAC providing a DC signal, thus allowing the use of a slow low-power device. Positive and negative DC voltage is, in the suggested design, further divided passively into four analog levels representing one quarter of the waveform. Two 8:1 multiplexers are combining the positive and negative voltages to generate a stepwise sine waveform with the tick frequency of 1,6 MHz. The multiplexer switching and enable / disable control is made by the 4-bit counter controlled by the 1,6 MHz clock. Note that the series resistance of the multiplexer switch is largely affected by the temperature variation and the voltage level being switched. In order to keep the injection amplitude stable with temperature variation, the switch current shall be minimized, which is achieved by the buffer amplifier following the multiplexers.

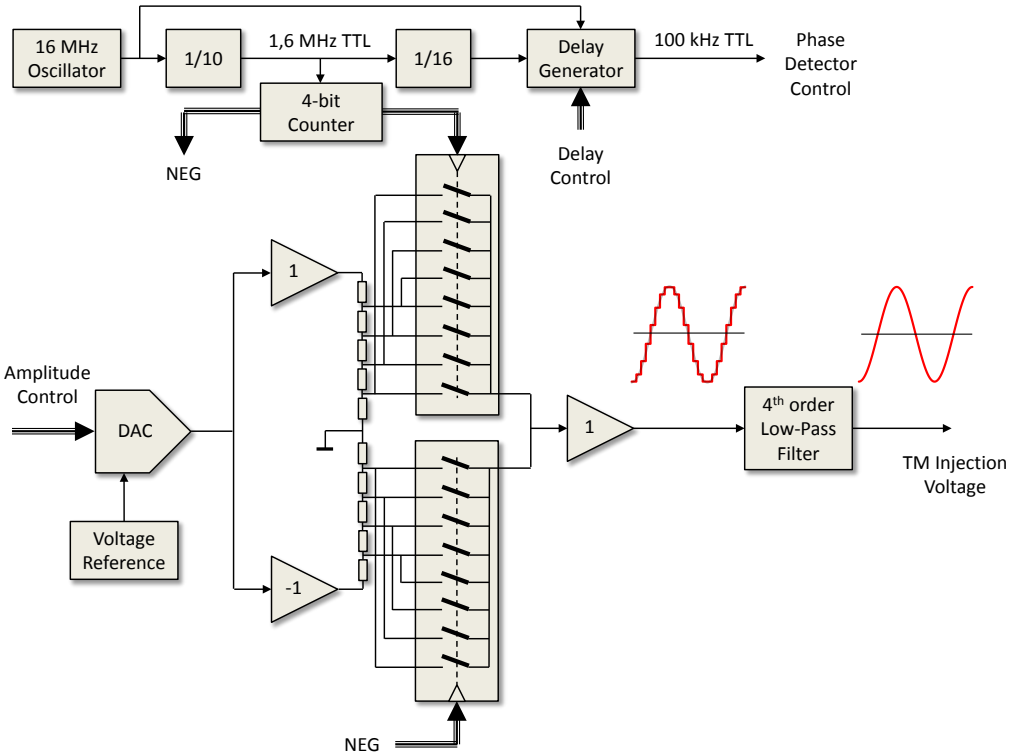

Figure 2-19 TM injection signal generated from a 1,6 MHz stepwise sinusoidal waveform using lower order low-pass filtering to remove harmonics shifted to higher frequencies

Regarding the multiplexer, instead of the suggested schematic, one 16:1 chip or four chips containing quad independent switches could be used to widen the range for selection of the parts with space heritage. The most important parameter is the settling time of the analog switch that should be maximum 200 ns compared to the selected 625 ns switching period (1,6 MHz). Preference shall be given also to the chips with lower charge injection, e.g., around 5 pC, to reduce glitches at the switching events. Note that the switch ON resistance level and its variation with the input voltage level are not important if the switch current is made negligible. One possible variation of this circuit would be with different DAC control, e.g., such to generate a squared bipolar waveform at 100 kHz instead of a DC voltage. This would make one multiplexer and the inverter obsolete, but would require a DAC almost as fast as the multiplexer.

The following multiplexer / switches operating in the military (MIL) temperature range could be used:

Table 2-10 Analog switches and multiplexers suitable for the injection waveform generator

Part number	Manufacturer	Type	Speed	Charge Injection	Switch resistance	Power
ADG506	Analog Dev.	16 : 1	200 ns	4 pC	280 Ω	10 mW
DG406	Maxim	16 : 1	110 ns	2 pC	60 Ω	1,2 mW
MAX396	Maxim	16 : 1	150 ns	2 pC	60 Ω	10 µW
DG408	Maxim	8 : 1	115 ns	2 pC	60 Ω	1,2 mW
ADG201HS	Analog Dev.	4	50 ns	10 pC	50 Ω	240 mW

2.6.2 Low-Pass Filtering

According to the Fourier series of the square wave (2.61), a square wave can be constructed from the infinite numbers of odd harmonics with amplitudes of $4A/(\pi i)$, where A is the amplitude of the square wave and i is the harmonic number.

$$f(t) = A\frac{4}{\pi}\sum_{i=1,3,5,\ldots}^{\infty}\frac{sin(\omega t)}{i} \tag{2.61}$$

Because the 300 kHz harmonic (i =3) is very large (4,24 V for A = 10 V), it must be strongly attenuated, thus requiring a large order of low-pass filtering.

2.6.2.1 Initial filter design

As proposed in Figure 2-18, four second order Butterworth filters are used. Each second order filter with corner frequency at 100 kHz attenuates the third harmonic only by approximately 19 dB. In total, it can attenuate the 300 kHz harmonic to the level of 670 µV for the maximum 10 V injection square wave, which is still considerably large.

A slightly modified filtering scheme for the square waveform could be implemented as follows: two filters at the corner frequency of 50 kHz e.g., to add additional attenuation at 300 kHz, followed by two more filters at a corner frequency close to 100 kHz, but with much smaller damping, e.g., ξ = 0,12, to regain the loss in amplitude at 100 kHz. This scheme would reduce the third harmonic to about 50 µV, i.e., a 13-time reduction. While this would be satisfactory, the 0,12 damping is causing 12 dB (4 times) gain peaking. One could therefore expect a gain variation between different operational amplifiers (with a different slew rate) and much larger filter gain sensitivity to temperature. The latter is due to the very sharp phase change at 100 kHz, which would cause a larger phase fluctuation when filter parts are affected by the temperature. Fluctuating phase of the injection waveform would reduce the sensing demodulator output, which is tuned to a nominal phase delay at a certain temperature. This larger filter temperature sensitivity would mask the through sensing low-frequency performance.

2.6.2.2 Suggested filter design

The harmonics of the square wave, discussed in the previous section, and the harmonics of the suggested stepwise waveform are shown in Figure 2-20. The main benefit of the latter is that higher harmonics appear first at 1,5 MHz, thus allowing easier rejection. From [28] the higher harmonics appear at

$$h = 4 \cdot m \cdot i \pm 1 \tag{2.62}$$

where h is the number of the higher harmonics, which exists in the spectra, m is number of approximation levels (in our case m = 4) and i = 1, 2, 3, …. The sine waveform approximation or quantization levels are determined [28] by

$$g_q = G_0 \cdot sin\left[\frac{\pi}{4m}(2q-1)\right] \tag{2.63}$$

where G_0 is the amplitude of the sine waveform and q = 1, 2, … m. In the suggested 4-step approximation, the g_1 to g_4 levels of unity injection sine waveform are 0,1951, 0,5558, 0,8315 and 0,9808. For the 10 V sine waveform the amplitude of harmonics is simply G_0/h, i.e., 10/15, and 10/17 for the first two higher harmonics, as shown in Figure 2-20.

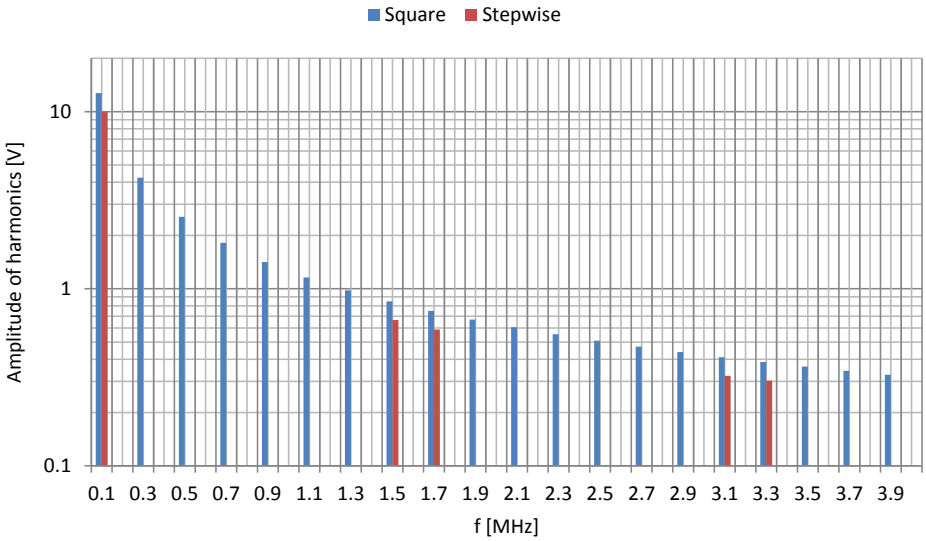

Figure 2-20 Amplitude of harmonics for 10 V square and stepwise waveforms

A piecewise waveform shown in Figure 2-21, i.e., a linear approximation between the discrete defined levels, would cause a further reduction of the harmonics [29].

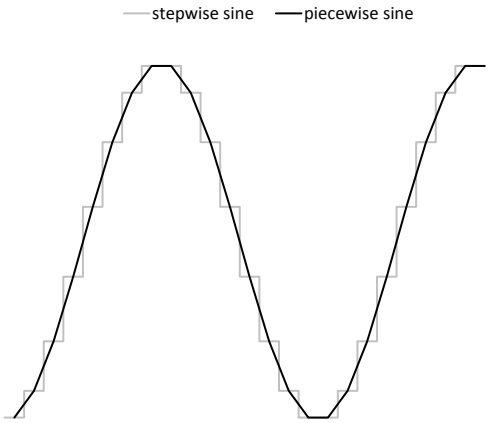

Figure 2-21 Stepwise and piecewise sine waveform with 4-level approximation

This approach requires additional integration of the stepwise waveform. Since the integration is a linear process, the spectral content remains the same as for the stepwise waveform. The benefit is that the attenuation follows the G_0/h^2 rule, which brings 15 times more attenuation of the 1,5 MHz harmonic. This improvement is not necessary in our application, as will be seen later in the analysis.

With the first higher harmonic at 1,5 MHz, it is enough to implement the 4th order low-pass filter. With two identical 100 kHz filters with damping of ξ = 0,5 to maintain the unity gain at 100 kHz, the first higher harmonic of the 10V injection waveform would be attenuated 94 dB, i.e., from 667 mV to 13,3 µV. The 10V piecewise waveform would have its 1,5 MHz harmonic of 45 mV attenuated to 0,9 µV.

The sensing band-pass filter, which will be analyzed in 2.9, will have its bandwidth of several tens of kHz (e.g. ±30kHz) around the 100 kHz central frequency. It would thus further attenuate the stepwise 1,5 MHz harmonic by 44 dB (2^{nd} order filter), i.e., to 0,08 µV. The signal will then be further treated by the synchronous phase detector of only ±5Hz bandwidth, which would finally reject, by another 2^{nd} order filter, all out-of-band frequency components. Therefore, it can be concluded that the piecewise waveform is an unnecessary design complication for the IS-FEE design.

2.6.3 Expected Performance

The preferred voltage reference and the list of possible multiplexer parts are provided in 2.5.3 and Table 2-10, respectively. In the injection waveform generator, the most critical parts affecting the noise performance are the 16-bit DAC and the operational amplifier, which is inverting the DAC output for the multiplexer. The amplifiers of the low-pass filtering section are AC coupled at the end and thus cannot affect the low-frequency noise.

2.6.3.1 DAC performance

With the DC DAC output scheme, the DAC code never changes once it has been set and therefore, its speed (settling time) is not critical. The most important parameter is the noise of the DAC analog output consisting of an internal buffer and possibly an internal voltage reference. There are not many 16-bit DACs with space heritage, especially not at low power. Two possible parts from Analog Devices in the MIL operating range are suitable, having equal characteristics (Table 2-11) and differing only in the type of the digital interface. These are AD669 [30] with a parallel and the AD660 with a serial interface, both having an internal voltage reference and an input for external reference. The settling time of these converters is about 8 µs, which means that they can only operate as a DC source in the selected application. Also provided in Table 2-11 are the 7846A space-qualified, radiation hardened (100 krad) DAC from Maxwell and its equivalent commercial part AD7846 from Analog Devices. They have much larger 1/f noise, so the preference is given to AD660/669.

Table 2-11 The DAC characteristics (typical values) at ±10 V full scale range and with internal voltage reference

Part number	Ref. noise at 1 kHz	Ref. noise at 1 Hz	Ref. temp. sensitivity	DAC noise at 1 kHz	DAC noise at 1 Hz	Power
AD660 / AD669	$125\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$160\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$15\,\frac{\mathrm{ppm}}{\mathrm{K}}$	$120\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$800\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	365 mW
7846A / AD7846	External voltage reference			$50\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$4800\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	100 mW

Note that the AD660/669 DAC noise in this table does not include the voltage reference noise, but its noise can be extrapolated from the total low-frequency 1/f noise. The internal reference noise, the DAC internal buffer noise and the DAC total noise can be modeled by

$$\begin{aligned} S_{\mathrm{DAC_R}}^{1/2} &= 0{,}0125\,\frac{\mathrm{ppm}}{\sqrt{\mathrm{Hz}}} + \frac{0{,}01\ \mathrm{ppm}}{\sqrt{f}} \\ S_{\mathrm{DAC_B}}^{1/2} &= 0{,}012\,\frac{\mathrm{ppm}}{\sqrt{\mathrm{Hz}}} + \frac{0{,}079\ \mathrm{ppm}}{\sqrt{f}} \\ S_{\mathrm{DAC}}^{1/2} &= 0{,}0173\,\frac{\mathrm{ppm}}{\sqrt{\mathrm{Hz}}} + \frac{0{,}08\ \mathrm{ppm}}{\sqrt{f}} \end{aligned} \tag{2.64}$$

where $S_{\mathrm{DAC_R}}^{1/2}$ is the internal reference, $S_{\mathrm{DAC_B}}^{1/2}$ is the internal buffer and $S_{\mathrm{DAC}}^{1/2}$ the total DAC relative noise ASD normalized to 10 V output range. The noise density for the reference and the DAC at 0,1 mHz, calculated from (2.64), are $1\ \mathrm{ppm}/\sqrt{\mathrm{Hz}}$ and $8\ \mathrm{ppm}/\sqrt{\mathrm{Hz}}$, respectively.

The AD660/669 DAC internal reference appears to be better than the LT1021 reference having 4 times less noise at 0,1 mHz, but this needs to be verified, as the data sheet [30] provides very limited information of noise below 1 Hz. In addition, the DAC internal reference has temperature sensitivity about 3 times worse than the sensitivity of LT1021

(typically 3 ppm/K). On the LPF and LISA missions the temperature stability of the electronics mounting interface will be very high, around $0{,}1\,\mathrm{K}/\sqrt{\mathrm{Hz}}$ at 0,1 mHz. Therefore, this level of temperature fluctuation will influence the DAC internal voltage reference and cause an equivalent DAC noise of $15\,\mathrm{ppm/K} \cdot 0{,}1\,\mathrm{K}/\sqrt{\mathrm{Hz}} = 1{,}5\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$. This noise is similar to the inherent internal reference noise at 0,1 mHz ($1\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$) and well inside the $30\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ limit shown in Figure 2-16. From this analysis it appears that the AD660/669 DAC internal reference would also be compatible with the requirements.

The noise of the space qualified 7846A DAC is $15\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ at 1 mHz and $48\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ at 0,1 mHz. Comparing the noise limits shown in Figure 2-16, it can be concluded that this part would satisfy requirements of the LPF mission (1 mHz) and be marginally compliant with the requirements of the LISA mission (0,1 mHz). A very fast 16-bit DAC that could also be used is the space-qualified, 100 krad radiation tolerant part AD768S from Analog Devices. The parameters of the commercially available equivalent part AD768 [31] are given in Table 2-12.

Table 2-12 High-speed, space qualified 16-bit DAC

Part number	Settling	Reference	Ref. temp. sensitivity	Output	DAC noise into 50 Ω	Power
AD768S / AD768	25 ns	INT / EXT	$30\,\frac{\mathrm{ppm}}{\mathrm{K}}$	CURRENT	$3\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	465 mW

This part could be used as the direct sine waveform synthesizer (e.g., at 16 MHz), thus replacing the multiplexers and driving directly an output buffer followed by ≥ 100 kHz low-pass filters. To comply with the waveform amplitude stability performance, an external voltage reference is suggested instead of the internal one. The DAC low-frequency noise is not important, as this DAC would operate in AC mode. With the additional power of the digital circuits operating at a high frequency, this solution is currently not the preferred one.

2.6.3.2 DC amplifier performance

According to Figure 2-19, two buffers will be used to buffer and invert the DAC output. Their performance is crucial for performance at a low frequency, as they operate in DC mode. The following parts come as potential precision DC buffers or inverters with the important noise characteristics shown in Table 2-13.

The last two parts are the auto-zero / zero-drift amplifiers with effective 1/f noise cancellation for which the corner frequency is not applicable (N/A). The OP77 and these two auto-zero amplifiers are the true space-qualified parts. The OP97 part has space heritage, but is not space-qualified.

The requirements for the amplifier shall be set in relation to the DAC performance at the lowest injection amplitude of interest. The DAC output noise scales down with the reduction of the output amplitude. The nominal injection amplitude is about 4,8 V peak, which is attenuated on the TM via capacitive coupling to 0,6 V peak, as explained in 2.6. During testing, a special TM simulator is used for which direct application of 0,6 V voltage is needed. Hence, the 0,6 V peak level is taken as the minimum DAC voltage of interest.

Table 2-13 Precision operational amplifiers suitable for the injection waveform generator

Part number	Manufacturer	Voltage noise at 1 kHz	Voltage noise at 1 Hz	1/f noise corner frequency	Offset temp. sensitivity	Power
OP77	Analog Dev.	$9{,}6\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$12{,}5\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	0,7 Hz	$0{,}5\,\frac{\mu\mathrm{V}}{\mathrm{K}}$	50 mW
OP97	Analog Dev.	$14\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$22\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	2,5 Hz	$0{,}1\,\frac{\mu\mathrm{V}}{\mathrm{K}}$	12 mW
LM6172	National	$12\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$40\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	10 Hz	$6\,\frac{\mu\mathrm{V}}{\mathrm{K}}$	69 mW
AD8629	Analog Dev.	$22\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$22\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	N/A	$0{,}002\,\frac{\mu\mathrm{V}}{\mathrm{K}}$	4,5 mW
LMP2012	National	$35\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$35\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	N/A	$0{,}015\,\frac{\mu\mathrm{V}}{\mathrm{K}}$	5 mW

With $8\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ DAC, relative noise at 0,1 mHz (2.64) and its output voltage of 0,6 V, the voltage noise limit applicable to the operational amplifiers at 0,1 mHz is at most $4{,}8\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$. Table 2-14 shows calculated noise levels at 0,1 mHz for all selected amplifiers.

Table 2-14 Low-frequency noise density of precision amplifier candidates

	Limit	OP77	OP97	LM6172	AD8629	LMP2012
Voltage noise at 0,1 mHz	$4{,}8\,\frac{\mu\mathrm{V}}{\sqrt{\mathrm{Hz}}}$	$0{,}8\,\frac{\mu\mathrm{V}}{\sqrt{\mathrm{Hz}}}$	$1{,}9\,\frac{\mu\mathrm{V}}{\sqrt{\mathrm{Hz}}}$	$3{,}8\,\frac{\mu\mathrm{V}}{\sqrt{\mathrm{Hz}}}$	$0{,}03\,\frac{\mu\mathrm{V}}{\sqrt{\mathrm{Hz}}}$	$0{,}04\,\frac{\mu\mathrm{V}}{\sqrt{\mathrm{Hz}}}$

Although the auto-zero amplifiers are the clear winners of this competition, one should note that they are unipolar 0 to 5 V power supply parts, while the other operate at bipolar ±15 V supply. To achieve ±10 V levels with these unipolar parts, one should implement the composite amplifier architecture like the one suggested in [32]. The OP77 [33] is also an acceptable part for this application.

2.6.3.3 AC amplifier performance

Many operational amplifiers can be used for the AC buffering, i.e., to cancel the multiplexer switching current and for the low-pass filtering of the 100 kHz injection waveform. The low-frequency performance is less important (AC mode). Instead, a larger slew rate and bandwidth are of interest. A considerable number of space-qualified parts exist from various manufacturers, as shown in Table 2-15. Note though that the AC amplifier in the trans-impedance application (2.8.2) would, furthermore, need a very low current noise, preferably at the $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ level, i.e., the amplifier with the FET input stage.

The last two amplifiers are commercial parts with similar characteristics that can also be used for prototyping. The presented power is for the single amplifier and it is obvious that it plays an important role for the electronics design. For power-saving purposes it would be beneficial to operate the front stage at ±5 V and only the last amplifier at ±15V.

Note that the RH1056 (equivalent commercial part LT1056) and OPA627 are the amplifiers with FET input stage. The current noise for the OPA627 is shown for the 100 Hz, since data at higher frequencies are not given in the data sheet.

Table 2-15 High-speed operational amplifiers suitable for the AC operational mode

Part number	Manufacturer	Voltage noise at 1 kHz	Current noise at 1 kHz	Slew rate	Bandwidth	Power (±15 V)
LM6172	National	$12\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$1\,\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$	$3000\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	100 MHz	69 mW
OP467S / OP467	Analog Devices	$6\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$0{,}8\,\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$	$125\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	28 MHz	240 mW
RH1056A / LT1056	Linear Technology	$14\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$1{,}8\,\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$	$16\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	6,5 MHz	150 mW
RH1498 / LT1498	Linear Technology	$12\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$0{,}3\,\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$	$6\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	10,5 MHz	54 mW
LT1355	Linear Technology	$10\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$0{,}6\,\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$	$400\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	12 MHz	30 mW
OPA627[6]	Texas Instruments	$5{,}2\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$1{,}6\,\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$	$55\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	16 MHz	210 mW

With the previously set requirement of $4{,}8\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ and the fact that the filtering amplifiers operate at unity gain, their (white) noise above 1 kHz at $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ scale will be negligible when down-converted from 100 kHz to the measurement bandwidth.

The highest slew rate for the sine waveform of 100 kHz at zero crossing is 6,28 V/µs at the maximum injection signal of 10 V peak. Therefore, the LM6172 [34] seems to be a good compromise between noise, speed and power. The RH1498 (equivalent commercial part LT1498 [35]) would be marginally compliant in view of the slew rate, but only for the maximum signal level.

2.7 Differential Transformer

The sensing differential transformer (the sensing bridge) is the most important part of the sensing chain responsible for the noise performance, both at high frequency (1 Hz) due to its thermal losses and low frequency (0,1 mHz) due to fluctuation of its parameters. The purpose of the transformer is the sensing of differential currents generated by movement of the TM between electrodes.

Previous transformer development by UTN is described in [12], [16] and [36]. Several transformers were built using MnZn N26 ferrite material with high permeability $\mu \approx 2300$ and low $tan\ \delta < 0{,}01$ from Siemens Matsushita Corp. (currently EPCOS AG). The main characteristics achieved are provided in Table 2-16.

Table 2-16 Characteristics of the differential transformer made by UTN

Core shape	Inductivity	No. of turns	Quality factor Q	Stray capacitance	Inductance imbalance	Imbalance stability
RM8	4,98 mH	41	150-180	12 pF	100 ppm	$2\,\frac{\mathrm{ppm}}{\sqrt{\mathrm{Hz}}}$

The inductance imbalance stability (last column) is shown for the 0,1 mHz and was dominated by the poor temperature isolation of the circuit. The N26 material is now obsolete

[6] The current noise is specified at 100 Hz. In fact, much larger $335\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ current noise at 100 kHz has been measured during testing of the sensing circuit (see 4.3.1.1)

and was replaced in 2002 by N45 and N48. According to the manufacturer, the N26 was used for the broadband transformers and is now replaced by N45 for this application. More interesting is the new N48 material, used for high *Q* inductors in resonant circuits and filters. The advantages of N48 are higher saturation flux density, higher Curie temperature and lower temperature dependence of the initial permeability, the last being the most important. It also has a comparable relative loss factor and identical initial permeability as the N26 material.

By dividing the inductivity by the square of the number of turns, one can calculate the inductance factor relative to the number of turns $N = 1$, the A_L value:

$$A_L = \frac{L}{N^2} = \frac{4{,}98\ mH}{41^2} = 2963\ nH \tag{2.65}$$

From the old data sheet for N26 material and from (2.65) it can be concluded that UTN used the ungapped core with $A_L = 2900^{+30}_{-20}$ nH. This will be important for further analysis. The transformer core size used in the UTN experiment is also useful information for the analysis. The RM8 core has a diameter of 23 mm and a height of 17 mm.

2.7.1 Design Drivers

The transformer design is constrained by the capacitance noise of the single sensing channel (2.30), which can be rewritten as

$$TDS = {f_0}^3 LQ \geq \frac{8k_B T}{(2\pi)^3 \left(U_M S_{\Delta C}^{1/2}\right)^2} \tag{2.66}$$

where *TDS* is the transformer design solution, f_0 is the resonant frequency and *L* and *Q* are the main transformer parameters. The remaining parameters from (2.66) are fixed: Boltzmann constant $k_B = 1{,}38 \times 10^{-23}\ \mathrm{m^2 kgs^{-2}/K}$, temperature $T = 300$ K (27ºC), TM injection voltage $U_M = 0{,}6$ V peak and the required sensing capacitance noise $S_{\Delta C}^{1/2} = 1\ \mathrm{aF}/\sqrt{\mathrm{Hz}}$ (Table 2-7). Using the above values, (2.66) can be simplified to

$$TDS = {f_0}^3 LQ \geq 3{,}709 \times 10^{14}\ \frac{H}{s^3}$$
$$LQ \geq 0{,}37\ H \quad \text{for } f_0 = 100\ \text{kHz} \tag{2.67}$$

As already discussed in 2.1.2, the enlargement of the resonant frequency f_0 has the largest positive impact on noise reduction, but there are also limits in the electronics design. Higher frequencies require faster multiplexer for the TM injection voltage generator. The 300 kHz injection frequency would require a multiplexer control frequency of 4,8 MHz (208 ns) and thus maximum 100 ns multiplexer switching. The switching characteristics of available multiplexer parts (Table 2-10) make higher injection frequencies than 300 kHz impractical. Finding a maximum for *TDS* is difficult because *L* and *Q* are at odds – one can achieve a large *L* at a lower *Q* and vice versa. A larger frequency will further reduce *Q* because the losses of the ferrite material enlarge by the frequency. The options can be evaluated by changing three parameters of *TDS*.

To include 50% design margin, a *TDS* twice as large is set. A summary of possible design solutions with this margin is provided in Table 2-17 and Table 2-18.

Table 2-17 Transformer design solutions for frequencies between 60 kHz and 120 kHz

f	60 kHz			80 kHz			100 kHz			120 kHz		
LQ	3,434 H			1,449 H			0,742 H			0,429 H		
L/mH	6	7	8	3	4	5	3	4	5	2	3	4
Q	572	491	429	483	362	290	247	186	148	215	143	107

Table 2-18 Transformer design solutions for frequencies between 150 kHz and 300 kHz

f	150 kHz			200 kHz			250 kHz			300 kHz		
LQ	0,220 H			0,093 H			0,047 H			0,027 H		
L/mH	1	2	3	0,6	0.8	1	0.4	0.6	0.8	0.3	0.4	0.5
Q	220	110	73	155	116	93	118	78	59	90	68	54

Some initial conclusions can be drawn from the above:

- At lower frequencies, achieving a quality factor Q larger than 500 is very difficult and thus it is better to maximize inductance L. This would require a larger transformer core
- At higher frequencies, Q and L do not need to be large and thus the transformer could be smaller

Before selecting a design, one must first analyze the ferrite material. Design solution tables will later serve as guidelines for selecting the proper inductance. Even though the resonant frequency can be tuned with the proper capacitance for any selected inductance, the goal is to operate the bridge with the maximum achievable inductance (and *TDS*) and thus reduce the noise as much as possible.

2.7.2 Transformer Core Selection

The ferrite materials used for resonant circuit inductors are characterized by a low relative temperature coefficient and a low relative loss factor, which makes these inductors stable and allows achieving a large Q. Several materials falling into this category are given in Table 2-19.

Table 2-19 Characteristics of the ferrite MnZn materials suitable for the sensing transformer

Material	Manufacturer	μ_i - initial permeability	Frequency range /MHz	$tan\ \delta/\mu_i$ - relative loss factor $/10^{-6}$	α_F - relative temp. coeff. /ppm/K
N26	EPCOS	2300	0,01 – 0,1	< 2,8 (10 kHz) < 3,8 (100 kHz)	0 – 1,5
N48	EPCOS	2300	0,01 – 0,1	< 4 (10 kHz) < 6 (100 kHz)	0,3 – 1,3
3B7	Ferroxcube	2300	≤ 0,1	< 5 (100 kHz)	±0,6
3H3	Ferroxcube	2000	≤ 0,2	< 2,5 (100 kHz)	0,4 – 1
3D3	Ferroxcube	750	0,2 – 2	< 10 (300 kHz)	0,5 – 2,5
M33	EPCOS	750	0,2 – 1	< 12 (200 kHz) < 20 (1 MHz)	0,5 – 2,6

The 3D3 and M33 are higher frequency materials and also have a higher temperature sensitivity. The obsolete N26 material, used in the previous design, is also shown for

comparison. Even though the maximum suggested frequency for certain materials is 100 kHz, they can be used at higher frequencies, but with higher losses.

2.7.2.1 Quality factor

To properly compare losses, it is better to convert the relative losses $tan\ \delta/\mu_i$ into absolute losses and then into the quality factor *Q by*

$$tan\ \delta = \frac{tan\ \delta}{\mu_i} \cdot \mu_i = \frac{1}{Q} \tag{2.68}$$

which is then summarized for different frequencies in Table 2-20.

Table 2-20 Quality factors of the ungapped ferrite materials at different frequencies

Q (f)	N26	N48	3B7	3H3	3D3	M33
60 kHz	135	115	329[7]	3337	-	-
100 kHz	115	106	230	200	1887	163
200 kHz	62	70	119	73	1567	135
300 kHz	27	36	68	36	133	114

The quality factor is derived either from the curves of relative losses or the curves of complex permeability shown for the N48 [37] and M33 material in Figure 2-22, respectively. In case of complex permeability, the (absolute) loss factors *tan δ* and *Q* are calculated from the real part μ_S' (representing inductance) and imaginary part μ_S'' (representing losses) of the complex permeability $\bar{\mu} = \mu_S' - j\mu_S''$ by

$$tan\ \delta_S = \frac{\mu_S''}{\mu_S'} = \frac{R_S}{\omega L_S} = \frac{1}{Q} \tag{2.69}$$

where subscript *S* stands for series inductance model with resistance R_S and inductance L_S.

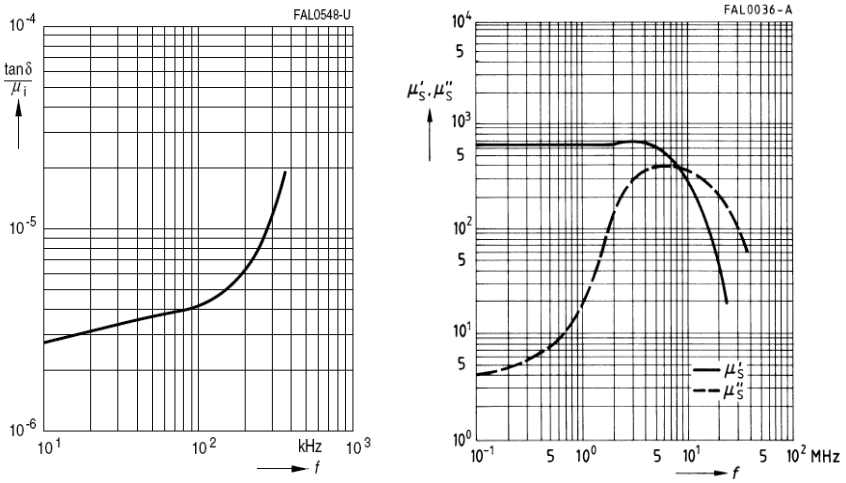

Figure 2-22 Relative losses of N48 material (left) and complex permeability of M33 material (right) as a function of frequency

Note that the quality factors calculated in Table 2-20 are for ungapped cores. It will be shown later that the use of gapped cores improves temperature stability and reduces the losses. The characteristics of the candidate materials provided in Table 2-19 and Table 2-20 lead to the following conclusions:

[7] These data are extrapolated by extending the curves from the data sheet and thus have lower accuracy

- The 3B7 and 3H3 materials have the highest *Q* between 60 kHz and 100 kHz
- The 3D3 and M33 materials have a higher *Q* for 200 kHz and 300 kHz operation, but also a higher sensitivity to temperature
- Unfortunately, all three Ferroxcube ferrite materials, 3B7, 3H3, and 3D3, are currently only supported but not recommended for new designs. Furthermore, 3B7 material is available only in the form of a toroid, which is not favorable in our application due to open coil construction and thus larger electromagnetic interference (EMI)
- Therefore, only N48 and M33 materials from EPCOS are feasible options

Both ferrite core materials are available as RM and P – pot shapes, of which preference is given to the latter due to almost completely enclosed coil construction and thus the least generated EMI. In the previous design, UTN used an RM8 core to which a P26x16 size core would be comparable, i.e., approximately 26 mm in diameter and 16 mm in height, Figure 2-23.

Figure 2-23 RM (left) ferrite core used in the previous design and P (right) ferrite cores, the preferred solution for new design

Comparing the requested *Q* values (Table 2-17) with those of N48 and M33 at 100 kHz (Table 2-20), the N48 core has an inferior *Q*, e.g., the closest being 106 against the required 148 for 5 mH inductance. On the other hand, the M33 core has an adequate *Q* of 163.

Similarly, the same conclusion can be drawn by comparing Table 2-18 with the *Q* values at 200 kHz (Table 2-20), e.g., N48 with $Q = 70$ and M33 with $Q = 135$ against the required $Q = 93$ for 1 mH inductance.

Considering only the quality factor, this analysis gives preference to the M33 core, but the temperature stability of the M33 core is two times worse than that of the N48 core.

The cores that have air gap can significantly improve both parameters. The factor of improvement is the ratio between the effective and the initial permeability μ_e and μ_i, respectively. The effective permeability can be written as

$$\mu_e \cong \frac{\mu_i}{1 + \frac{s}{l_e}\mu_i} \tag{2.70}$$

where s is the air gap width and l_e is the effective magnetic path length for which $s << l_e$.

Another very important feature is that the value of the effective permeability of the gapped core, and thus the final transformer inductance, can be produced considerably more accurately than for ungapped cores, which have larger tolerances on the initial permeability, e.g., 3% and 30%, respectively. This would allow better reproducibility of the transformer parameters between sensing channels.

The effect of the air gap on the core loss factor $tan\ \delta$, the core temperature coefficient α and the inductance factor A_L can be written as

$$tan\,\delta_e = \frac{tan\,\delta}{\mu_i}\cdot\mu_e$$
$$\alpha_e = \alpha\frac{\mu_e}{\mu_i} = \alpha_F\cdot\mu_e = \frac{\Delta\mu_i}{\Delta T}\frac{\mu_e}{\mu_i} \tag{2.71}$$
$$A_L = \frac{L}{N^2} = \frac{\mu_0}{\sum\frac{l}{A}}\mu_e$$

where $tan\,\delta_e$ is the effective loss factor of the gapped core, α and α_e are the initial and the effective temperature coefficients of the ungapped and gapped cores, respectively, $\Delta\mu_i$ is the change in permeability due to the temperature change ΔT, μ_0 is the magnetic field constant and $\sum l/A$ is the magnetic form factor.

With a larger air gap the effective permeability is smaller, which proportionally reduces all three parameters in (2.71). Note that the reduction of A_L means that one must wind more turns on the gapped core to produce the same inductance compared to the ungapped core. This might require a larger core size.

2.7.2.2 Temperature coefficient

The gap size selection stems from the requirements for the acceptable core losses and temperature stability. The core losses have already been analyzed in 2.7.2.1, from which it is evident that the N48 core requires an improvement, i.e., a reduction of losses using the air gap. The requirement for the temperature stability will be derived from the temperature environment and the maximum sensing noise.

The influence of the temperature on the initial permeability and thus on the transformer inductance does not affect the sensing output to the first order because both transformer primary windings change inductance equally. The second-order effect arises from the non-zero initial (DC) imbalance of the inductance between two primary windings $(\Delta L/L)_{dc}$, which can fluctuate with the temperature and thus generate fluctuating sensing offset, i.e., a fictive TM movement.

In the sensing offset analysis the inductance in each transformer primary winding is defined by (A-4), which is rewritten below in the following form

$$L_{1,2} = L\left[1 \pm \frac{1}{2}\left(\frac{\Delta L}{L}\right)_{dc}\right] \tag{2.72}$$

The temperature influence on the inductance can thus be written as

$$L_{1,2}(T) = L(1+\alpha\cdot\Delta T)\left[1 \pm \frac{1}{2}\left(\frac{\Delta L}{L}\right)_{dc}\right] \tag{2.73}$$

After expansion and approximation of (2.73), the inductance of each primary winding and the relative inductance imbalance are

$$L_{1,2}(T) \cong L\left[1+\alpha\cdot\Delta T \pm \frac{\alpha\cdot\Delta T}{2}\left(\frac{\Delta L}{L}\right)_{dc}\right]$$
$$\frac{\Delta L}{L}(T) = \frac{L_1 - L_2}{L} \cong \alpha\cdot\Delta T\left(\frac{\Delta L}{L}\right)_{dc} \tag{2.74}$$

Therefore, in case of relative imbalance fluctuation, the temperature coefficient of the core is very much reduced by multiplication by the DC imbalance, which is a very small number.

Similarly, the fluctuation of the imbalance can be written from (2.74) as

$$S_{\Delta L/L}^{1/2} \cong \alpha \left(\frac{\Delta L}{L}\right)_{dc} S_T^{1/2} \tag{2.75}$$

where the temperature fluctuation of the electronics $S_T^{1/2} = 0{,}1\ \mathrm{K}/\sqrt{\mathrm{Hz}}$ at 0,1 mHz and the inductance imbalance $(\Delta L/L)_{dc} \leq 50\ \mathrm{ppm}$, as already specified in 2.6.3.1 and 2.3.2, respectively. The inductance imbalance fluctuation $S_{\Delta L/L}^{1/2}$ produces the sensing offset fluctuation according to (2.58), which can be written as

$$S_{x,\Delta L}^{1/2} \cong \frac{d}{4\sqrt{2}} S_{\Delta L/L}^{1/2} \leq \frac{1}{10} S_x^{1/2} \tag{2.76}$$

where it is required that the offset (position) fluctuation due to the inductance imbalance $S_{x,\Delta L}^{1/2}$ is 10 times smaller than the total position noise $S_x^{1/2}$. Note that the factor $\sqrt{2}$ in noise reduction comes from the combination of two sensing channels used to calculate translation and rotation, as defined by (2.37). In case of *x*-axis sensing gap of d = 4 mm and the total position noise requirement $S_x^{1/2} = 1{,}8\ \mathrm{nm}/\sqrt{\mathrm{Hz}}$, the maximum inductance imbalance fluctuation will be

$$S_{\Delta L/L}^{1/2} \leq 0{,}25 \frac{ppm}{\sqrt{Hz}} \tag{2.77}$$

Substituting (2.75) by (2.77) the minimum required core temperature coefficient is thus

$$\alpha \leq \frac{S_{\Delta L/L}^{1/2}}{S_T^{1/2} \left(\frac{\Delta L}{L}\right)_{dc}} \leq 0{,}05\ K^{-1} \tag{2.78}$$

This is definitely not a stringent requirement because even the ungapped cores can satisfy it. Specifically, from the relation between the absolute and relative temperature coefficient, α and α_F, i.e., $\alpha = \mu_i \cdot \alpha_F$ and the data given in Table 2-19, both N48 and M33 ungapped cores have their α negligible, i.e., 0,003 K^{-1} and 0,002 K^{-1}, respectively.

Even though the requirement for the temperature sensitivity can be satisfied with the ungapped core and, of course, even better with the gapped core, one can benefit from other characteristics of the gapped core. Namely, it will provide much more accurate permeability (inductance) and effective "amplification" of the quality factor. Using Table 2-17 and Table 2-18 as guidelines for 100 kHz and 200 kHz transformer design and the gapped core characteristics [38], the design solutions given in Table 2-21 seem feasible.

Table 2-21 The gapped core candidates with estimated characteristics – coil effects excluded

Size	P22x13		P26x16				P30x19		
Material	N48		N48			M33	N48		
f/kHz	100		100			200	100		
Tolerance	±5%		±3%	±3%	±5%	±3%	±3%	±3%	±5%
A_L/nH	1250		630	800	1000	160	630	1000	2000
μ_e	498		201	255	319	51	166	263	525
$\alpha_e/10^{-3}$ K^{-1}	0,65		0,26	0,33	0,42	0,14	0,22	0,34	0,68
Q_e	490		1213	956	764	1985	1469	927	464
L/mH	4	5	4	5	6	1	4	5	6
N of turns	57	63	80	79	77	79	80	71	107

Note that the M33 material is available only in a P26x16 core size and only for large gaps (small A_L values). While A_L and μ_e are provided on data sheets [38], the parameters α_e, Q_e and N are calculated by (2.71) using the parameters of the ungapped core given in Table 2-22.

Table 2-22 Parameters of the ungapped cores with requirements for 100 kHz and 200 kHz design solutions

	f/kHz	L	Q	Required Q	μ_i	$\alpha/10^{-3}$ K^{-1}	Required α/K^{-1}
N48	100	4 mH	106	≥ 186	2300 ± 25%	3	$\leq 50 \times 10^{-3}$
M33	200	1 mH	135	≥ 93	750 ± 25%	2	

By comparing the last two tables one can see the theoretical "amplification" of the quality factor Qe/Q and a reduction (improvement) of the temperature coefficient αe/α, both by roughly 4 to 14 times. The final quality factor will be reduced at least due to the winding losses, which is analyzed in 2.7.3. Since the winding scheme influences how many turns can be wound in a certain core volume, the final selection of the gap will be done after the analysis of the coil design. At this point, it appears that roughly 60 turns per winding are needed in a P22x13 core, 80 turns in a P26x16 core and up to 100 turns in a P30x19 core. The cores with 3% tolerance, highlighted in Table 2-21, are the favorite choices.

2.7.3 Transformer Coil Design

The core losses appear due to hysteresis losses, eddy-current and residual losses in the core material. The hysteresis losses are proportional to the peak flux, the hysteresis constant and the effective permeability of the core. In the sensing bridge application, the flux in the core is cancelled (TM is centered between electrodes) or very small due to a differential connection of the primary windings. Therefore, the hysteresis losses can be neglected. The eddy-current and residual core losses are proportional to the effective permeability and the relative permeability (2.71).

Losses in the coil are divided into winding losses due to the DC resistance of the wire, eddy-current losses in the wire and the electric losses in insulation. The DC resistance depends on wire length, cross-section area, material and the method of winding expressed by the space factor. The eddy-current losses in the winding are proportional to the frequency, the diameter of the wire, the dimensions of the coil former and core and the volume of conductor [39]. These losses will be analyzed in more detail in 2.7.3.1.

The voltage difference that exists between different coil parts produces the electrostatic field in the air and the dielectric (insulation) near the coil. The effect of the resulting storage of electrostatic energy can be approximated by a small capacitance between the coil terminals, called distributed capacitance. This capacitance, together with the inductance of the coil, produces a resonance that changes the inductance and the series coil resistance. The electric losses in insulation caused by this distributed capacitance are twofold: an increase in effective coil resistance due to the vicinity of the coil self-resonant frequency and additional dielectric losses that this distributed capacitance produces itself.

As a general rule, a maximum Q is obtained when the sum of the winding losses is made equal to the sum of the core losses. This is because the core losses are proportional to the effective permeability μ_e, while most of the winding losses are inversely proportional to μ_e [39]. Therefore, as an example, one must find the optimum core gap (optimum μ_e) to equalize the losses. The emphasis will be on reducing coil distributed capacitance.

Various winding techniques can reduce winding capacitance. A voltage gradient creates an electrostatic field, so separating turns with the greatest voltage will reduce the winding

capacitance. The dielectric constant of the material increases the capacitance by acting as a simple multiplier. The varnish, wire insulation and tapes having a dielectric constant greater than one increase the winding capacitance.

For the coil with the low frequency inductance L (i.e., measured at a low frequency) in series with the DC resistance R and both in parallel with the distributed capacitance C_d, the self-resonance occurs at

$$\omega_{SR} = \sqrt{\frac{1}{LC_d} - \left(\frac{R}{L}\right)^2} \cong \frac{1}{\sqrt{LC_d}} \tag{2.79}$$

where for small resistance the second term can be neglected. At resonance, the impedance is resistive and equal to

$$R_{SR} = \frac{L}{RC_d} \tag{2.80}$$

When the operating frequency approaches the self-resonant frequency, the coil inductance and the effective series resistance rise to their apparent values, which reduces the quality factor. This can be written as

$$\begin{aligned} L_{app} &= \frac{L}{1 - \left(\frac{\omega}{\omega_{SR}}\right)^2} \\ R_{app} &= \frac{R_{dc}}{\left[1 - \left(\frac{\omega}{\omega_{SR}}\right)^2\right]^2} \\ Q_{app} &= Q\left[1 - \left(\frac{\omega}{\omega_{SR}}\right)^2\right] \end{aligned} \tag{2.81}$$

It should be noted that when the frequency is at 20% of the self-resonant frequency, e.g., 100 kHz w.r.t 500 kHz, the Q_{app} is 96% of its original value. However, when frequency is at 70%, Q_{app} drops to 51% of its original value. It is therefore required that the self-resonant frequency be at least 400 kHz [23] for 100 kHz operation and 700 kHz for 200 kHz operation. In both cases, this would ensure that the Q_{app} is more than 90% of the initial Q. This means that the distributed capacitance must be limited by (2.79) to at most 40 pF for 100 kHz operation and an inductor of L = 4 mH. At 200 kHz operation and L = 1 mH, the distributed capacitance must be maximum 52 pF.

The distributed capacitance effects due to the coil self-resonance and the equivalent dielectric losses of the distributed capacitance itself, expressed as an additional equivalent coil series resistance R_d, can be written by [39]

$$R_d = \omega^3 L^2 C_d \left(\frac{2}{Q} + tan\ \delta_{Cd}\right) \tag{2.82}$$

where $2/Q$ represents losses due to the self-resonance and $tan\ \delta_{Cd}$ the dielectric losses in the wire insulation. The part representing self-resonant losses is an approximation using the Taylor series. The accurate formula follows from (2.81), as written below.

$$R_{d1} = R_{app} - R_{dc} = R_{dc}\left\{\frac{1}{\left[1-\left(\frac{\omega}{\omega_{SR}}\right)^2\right]^2} - 1\right\} \approx 2R_{dc}\left(\frac{\omega}{\omega_{SR}}\right)^2 = \frac{2\omega^3 L^2 C_d}{Q} \quad (2.83)$$

where Q is the quality factor assuming only DC resistance, i.e., $Q = \omega L/R_{dc}$ and ω_{SR} is calculated by (2.79). The formula for dielectric losses, i.e., the second part of (2.82), is given by Terman's Radio Engineer's Handbook [40] and the $tan\ \delta_{Cd}$ value can be found in [41].

$$R_{d2} = tan\ \delta_{Cd}\omega^3 L^2 C_d = tan\ \delta_{Cd}\omega L\left(\frac{\omega}{\omega_{SR}}\right)^2 = 0{,}0118\omega L\left(\frac{\omega}{\omega_{SR}}\right)^2 \quad (2.84)$$

where the $tan\ \delta_{Cd}$ value assumes the wire diameter to be larger than 0,125 mm.

2.7.3.1 Eddy current losses

The eddy current losses in a winding divide into the losses caused by the proximity effect and the skin effect, the former being much more important. The AC current in two round parallel wires is not distributed uniformly around the conductors. The magnetic fields from each wire affect the current flow in the other, resulting in a non-uniform current distribution, which, in turn, increases the apparent resistance of the conductors. In parallel round wires, this phenomenon is called the proximity effect. The tendency of a current to flow on the outside of a conductor at higher frequencies is called the skin effect. With the skin effect, the current distribution is affected by the conductor's own magnetic field, increasing the losses. The proximity effect is similar, the difference being that the mutual influence of multiple current carrying conductors causes uneven current distribution in the conductors, again increasing losses. This is illustrated in Figure 2-24 [42].

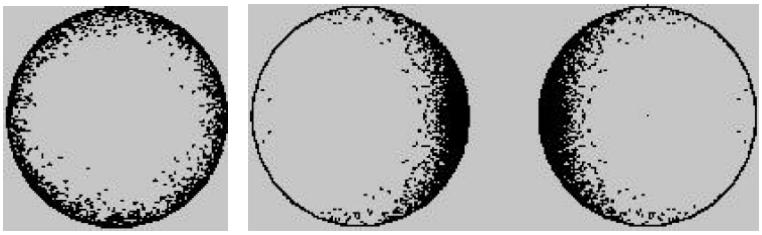

Figure 2-24 Current distribution for the skin effect (left) and the proximity effect (right) with current flow in the same direction

In the skin effect, less usable area for current flow increases the resistance and thus the winding losses. The skin depth δ or the conductor depth where the current drops to the level of $1/e \approx 0{,}37$ is for the copper conductor expressed by $\delta = 0{,}065/\sqrt{f}$.The depth is 0,21 mm and 0,15 mm at 100 kHz and 200 kHz, respectively. In 4.2.1 the transformer coil design has been optimized for the wire diameter of 0,15 mm. Since the wire radius (0,075 mm) is smaller than the above calculated skin depth, the skin effect will be negligible in the sensing bridge application (even for 200 kHz operation).

By definition, the skin effect does not change with winding construction. For proximity effect, multiple winding layers increase the magnetic field buildup and hence losses. Enlargement of the wire diameter can reduce skin effect losses but can usually further enlarge the proximity effect losses. Thinner wires are better for the multiple layer coil design [42].

It is difficult to derive an explicit formula for calculating the proximity effect and therefore, the calculation is usually made by simulation and by tweaking the model of eddy current losses with the real measurements. Modifications of initial simulation models are presented in [43] and [44] with the goal to improve the accuracy. To estimate the proximity effects in the

coil based on these models, one must first describe the baseline coil design shown in Figure 2-25.

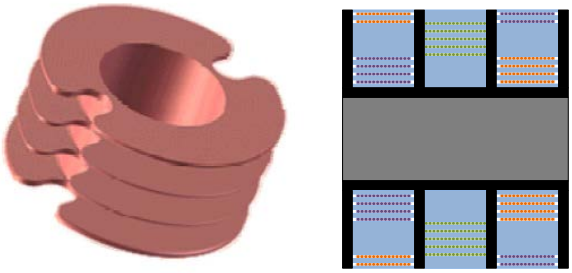

Figure 2-25 The P-core, 3-section, coil former (left) and the baseline coil design (right). Two primary windings are placed in the left and right sections and one secondary winding in the middle section

Based on Table 2-21, one possible coil solution would be to use the P26x16 size core / coil former and approximately 80 turns to achieve the required inductance. To ensure low stray capacitance between each primary winding and between the primary and secondary windings, the 3-section coil former is suggested, where each winding is wound in its own section, Figure 2-25.

Note that the primary windings are divided in two sub-windings that are crossed between sections to facilitate fine symmetry tuning, which is elaborated in 4.2.1. Each primary winding is made of 6 x 14 = 80 turns and the secondary winding of 5 x 16 = 80 turns. The turns of each winding layer are separated only by wire insulation, which is 0,02 mm for the suggested 0,15 diameter copper wire (0,17 mm external diameter). The layers are separated by a roughly 0,2 mm thick Teflon insulation. The primary sub-windings and the secondary winding are separated by a 1,6 mm thick insulation.

It is important to note that for the cores with large gaps (small μ_e and A_L) the stray field in the immediate vicinity of the air gap (middle section) can cause additional eddy current losses in the copper winding if the winding is too close to the gap. Therefore, it is advisable to put more insulation in this area. The second reason for the large insulation below the secondary winding is to ensure that the primary and secondary windings face each other only at the corners, thus minimizing the stray capacitance.

Table 2-23 summarizes the coil construction data, which are needed for the estimation of losses due to eddy currents.

Table 2-23 Differential transformer design parameters used for calculating winding losses

Parameter	Value
Wire (copper) diameter	d = 0,15 mm
Turn-to-turn separation (edge-to-edge, i.e. just insulation thickness)	v = 0,02 mm
Layer-to-layer separation (edge-to-edge)	h = 0,24 mm
Winding window breath (section width)	b_w = 2,9 mm
Turn-to-turn factor	v / d = 0,133
Layer-to-layer factor	h / d = 1,6
Number of layers	m_P = 6, m_S = 5
Number of turns per winding	N = 80
Length of each winding	l = 4,1 m
Operating frequency	f = 100 kHz

The power losses per (winding) unit length, derived in [44], when divided by the square of the current I, convert to an equivalent resistance per unit length R'_{ec} representing the additional AC resistance due to eddy current losses. R'_{ec} can be calculated by

$$R'_{ec} = \hat{G}\left(\frac{H}{I}\right)^2 \rho$$
$$\left(\frac{H}{I}\right)^2 = \frac{1}{3}\left(\frac{N}{b_w}\right)^2 \left(1 - \frac{1}{4m^2}\right) \tag{2.85}$$

where $\hat{G}$ is the unitless winding geometry parameter, H is the peak external sinusoidal magnetic field strength caused by currents in surrounding inductors and ρ is copper resistivity, $\rho = 1{,}68 \times 10^{-8}$ Ωm. It is important to note the effect of the magnetic field strength H, which is directly proportional to the eddy current losses. It is evident from (2.85) that the narrow (small) winding width b_w and the larger number of winding layers m increase losses. Note that for $m = 1$ the last factor in (2.85) is 0,75, but with $m = 2$ it is already 0,94. A design with more than two layers does not significantly increase losses, e.g., at $m = 6$, the factor is 0,993. Therefore, one should either use one layer and if not possible, it does not matter too much how many layers are used. Of course, since N gets larger with more layers, losses are further increased. The winding geometry, which models the proximity and the skin effect losses [43], is written by

$$\hat{G} = (1-w)k_1\sqrt{k_2}X\frac{sinh\left(\sqrt{k_2}X\right) - sin\left(\sqrt{k_2}X\right)}{cosh\left(\sqrt{k_2}X\right) + cos\left(\sqrt{k_2}X\right)} + w\hat{d}(X) \tag{2.86}$$

where w is the weighting coefficient, k_1 and k_2 are fitting coefficients, X is the skin depth factor and $\hat{d}(X)$ is the function used to smooth the curve that models $\hat{G}$. X and $\hat{d}(X)$ are further defined by

$$X = \frac{d}{\delta}$$
$$\delta = \sqrt{\frac{\rho}{\pi f \mu_r \mu_0}} = \frac{0{,}065}{\sqrt{f}} \tag{2.87}$$
$$\hat{d}(X) = \frac{0{,}096 \cdot X}{(X^{-3n} + b^{3n})^{n-1}}$$

where δ is the skin depth and b and n are tuning coefficients. The [43] provides the lookup table for all coefficients based on input coefficients v/d and h/d defined in Table 2-23. The closest input lookup table values are v/d = 0,1865 and h/d = 1,6587. The output coefficients of the lookup table are provided in Table 2-24.

Table 2-24 Proximity and skin effect coefficients for the actual coil design, v/d and h/d

k_1	k_2	b	n	w
1,6128	0,6015	0,2285	2	0,0117

Using parameters and coefficients from Table 2-23 and Table 2-24, the results of this analysis are provided in Table 2-25.

Table 2-25 Eddy current losses expressed as an additional AC coil resistance

X	$\hat{d}(X)$	$\hat{G}$	$\left(\frac{H}{I}\right)^2$	R'_{ec}	R_{ec}
0,7177	0,0255	0,0257	$2{,}5189 \times 10^8\ m^{-2}$	$0{,}1088\ \frac{\Omega}{m}$	0,446 Ω

To evaluate the importance of the eddy current losses, one must compare the above result with the DC coil resistance, which is calculated by

$$R'_{dc} = \frac{4\rho}{\pi d^2} = 0{,}9507\ \frac{\Omega}{\mathrm{m}}$$
$$R_{dc} = R'_{dc} \cdot l = 3{,}9\ \Omega \tag{2.88}$$

The AC resistance due to the losses is only 11% of the DC coil resistance and therefore, it can be concluded that for the baseline coil design the eddy current losses are low enough.

2.7.4 Expected Performance

A summary of the transformer losses is provided in Table 2-26.

Table 2-26 Transformer core losses and winding losses for 100 kHz operating frequency

	Core losses	Winding losses of 4 mH coil at 100 kHz				
Parameter	Q	R_{dc}	R_{d1}	R_{d2}	R_{ec}	R_{TOT}
Value	1213	3,9 Ω	0,537 Ω	1,854 Ω	0,446 Ω	6,737 Ω
Source	Table 2-21	(2.88)	(2.83)	(2.84)	Table 2-25	
Comment	For A_L = 630 nH	$Q_e = 644$	For f_{SR} = 400 kHz			$Q_e = 373$

The expected final quality factor of Q_e = 373 calculated by (2.14), in the worst case condition with the self-resonant frequency of only 400 kHz, would satisfy the quality factor goals stated in Table 2-22. With a higher self-resonant frequency, expected around f_{SR} = 600 kHz, the effective quality factor would rise to Q_e = 466. The losses are dominated by the DC resistance and the coil self-resonance as a consequence of distributed stray capacitance. In absence of all AC losses, the quality factor would be Q_e = 644.

Note that the optimum design would have equal core and winding losses, which is not the case in the proposed design. This is because the core and winding quality factors are 1213 and 373, respectively. Finding the optimum Q is not easy and some experimenting is needed. The guidelines for this optimization are summarized below [45]:

- Physically large cores provide a higher Q than physically small cores and the frequency at which this peak occurs is inversely proportional to the core size. That is to say, large cores produce a larger Q, but at a lower frequency
- At a certain core size, the frequency at which the peak Q values occur increases with decreasing permeability. That is to say, a core with a larger air gap produces a maximum Q at a higher frequency
- The frequency at which Q reaches its maximum decreases when the number of turns, and thus the inductance, increases

2.8 Preamplifier and Main Amplifier

An equally important part of the sensing chain, shown in Figure 2-15, is the AC amplifier. It consists of the preamplifier connected to the secondary winding of the differential transformer, followed by the main amplifier. The purpose of the preamplifier is to adapt and

amplify the differential transformer signal. This sinusoidal signal appears when the TM is off the center, and its amplitude represents the difference in capacitance generated by the TM and its surrounding electrodes. This differential capacitance thus describes the TM position from the center of the electrode enclosure.

There are several options in the preamplifier design: a single-ended or differential concept and instrumentation (voltage-to-voltage) or trans-impedance (current-to-voltage) amplifier type. In previous UTN development [16] a single-ended, trans-impedance amplifier (TIA) solution, using an integrated field effect transistor (FET) operational amplifier (op-amp) was first designed following the ONERA approach with the discrete charge amplifier [17]. Due to the unsatisfactory results caused by the problems with the asymmetric architecture (one transformer secondary terminal grounded), UTN modified the design by implementing a differential concept using an instrumentation amplifier. Although the amplifier performed well, it required constant tuning to the resonant frequency to stay with the constant gain. This will be addressed in the following section.

2.8.1 Instrumentation Amplifier

An instrumentation amplifier or just a high impedance differential buffer in the non-inverting amplifier configuration is shown in Figure 2-26. It amplifies the transformer output signal, which has maximum amplitude at the resonant frequency, as shown in Figure 2-6. Therefore, the amplifier output transfer function is expected to have a similar shape. The very stable electronics with respect to the temperature must be implemented to stay in this narrow band and thus to maintain the gain. That is the major problem with this solution.

Since the transformer output impedance is very large (> 500 kΩ), the input pull-down resistors, used to provide the ground path to amplifier's bias current, must also be very large. These resistors, which load the transformer output, and the resistors around the amplifier will set the gain of the circuit. The capacitors are used to implement the band-pass filtering.

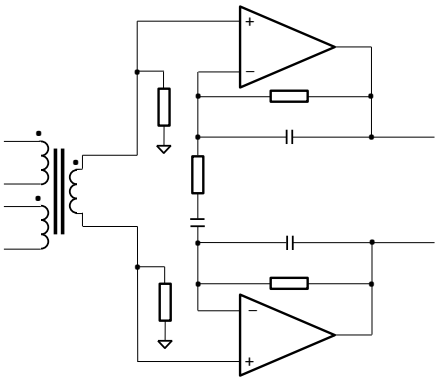

Figure 2-26 The AC instrumentation (buffer) amplifier solution for amplifying the voltage generated in the transformer secondary winding

2.8.2 Trans-Impedance Amplifier

The TIA is an inverting amplifier solution shown in Figure 2-27. It has the gain controlled by a single element, the small feedback capacitor in pF range. A large feedback resistor in MΩ range and a large decoupling capacitor in nF range, between the transformer and the amplifier, form a high-pass filter limiting the gain at low frequencies. The decoupling capacitor prevents the saturation of the amplifier at low frequencies close to DC by isolating the low transformer impedance (< 10 Ω). In addition, it attenuates the actuation frequencies and transients passing through the transformer to an acceptable level, as analyzed in 4.4.5.1.

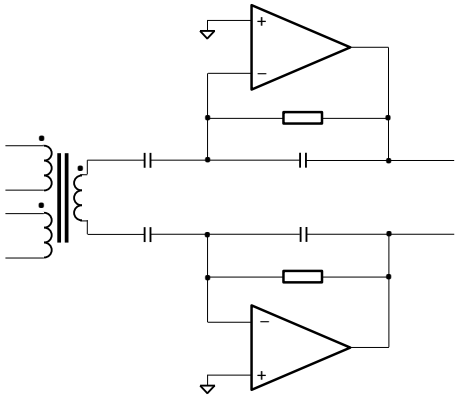

Figure 2-27 The trans-impedance amplifier (TIA) solution for converting and amplifying the current in the transformer secondary winding into voltage

To quickly examine features of two amplifier concepts, the electronics is simulated by the program *Micro-Cap* from Spectrum. The main advantage of the TIA circuit is a very flat shape of the transfer function around 100 kHz, which is illustrated in Figure 2-28, making this design less sensitive to the temperature variation. For this reason the TIA design has been selected as the preamplifier baseline solution. Furthermore, for the purpose of having a more symmetric design and a higher SNR, the differential TIA solution is suggested.

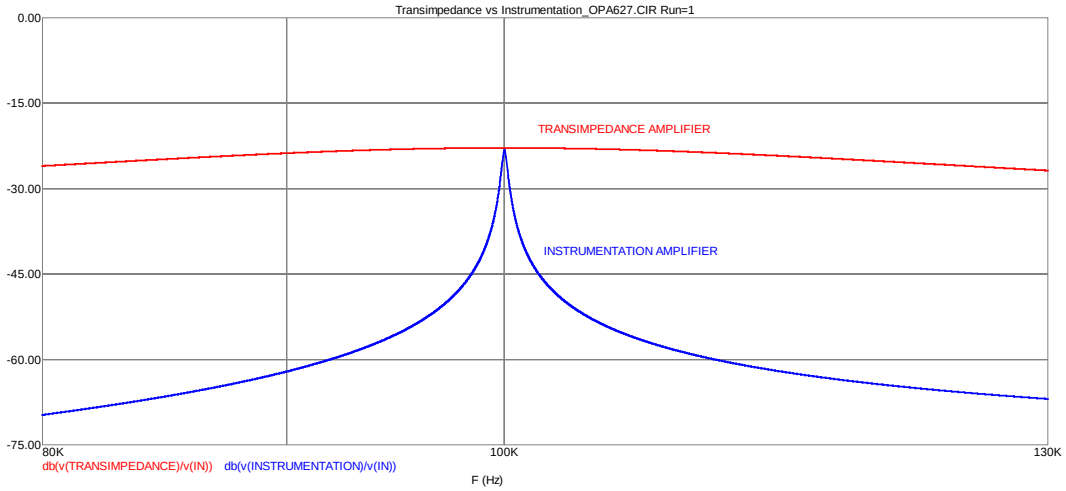

Figure 2-28 The transfer function (output voltage vs. TM injection voltage) of the TIA (red) and the instrumentation amplifier (blue) in the 80 kHz to 130 kHz frequency range. The gain at 100 kHz is around -23 dB for ΔC = 0,12 pF

Other differences between the two amplifier types are:

- The output phase, with respect to the TM injection voltage, is +90º for the instrumentation amplifier and -180º for TIA, with a very sharp transition for the former. The instrumentation amplifier would thus require constant readjustment of the phase delay in the demodulator
- The output noise spectrum density for TIA shows a shallow minimum at the operating frequency, while the instrumentation amplifier has a very sharp noise maximum at the same frequency, as shown in Figure 2-29

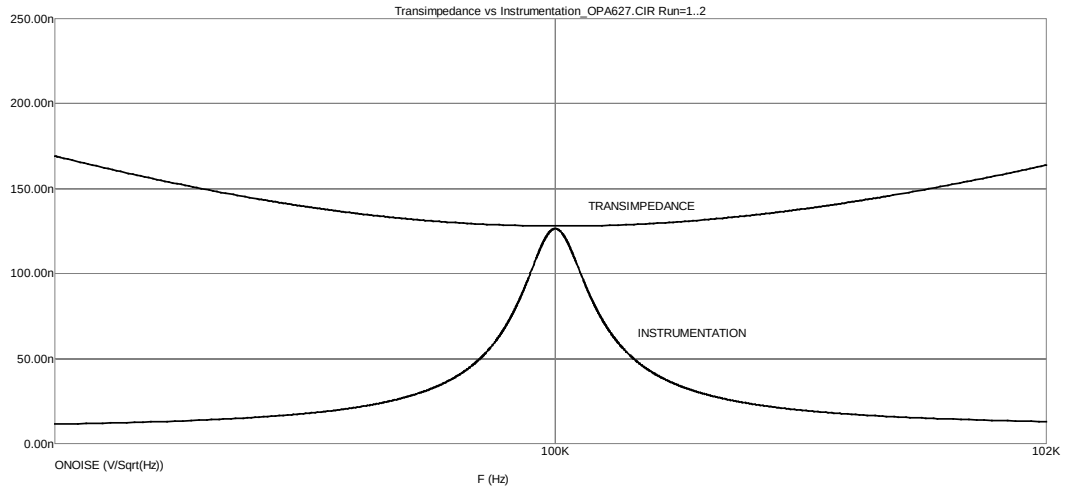

Figure 2-29 The noise spectrum density for the TIA (minimum) and the instrumentation amplifier (maximum) in the 100 kHz ± 2 kHz frequency range and 250 $nV/\sqrt{Hz}$ noise range

The gain flatness with TIA depends on the bandwidth of the operational amplifier, as it will be elaborated later during the mathematical modeling. Figure 2-30 illustrates this behavior by simulation of several amplifier candidates.

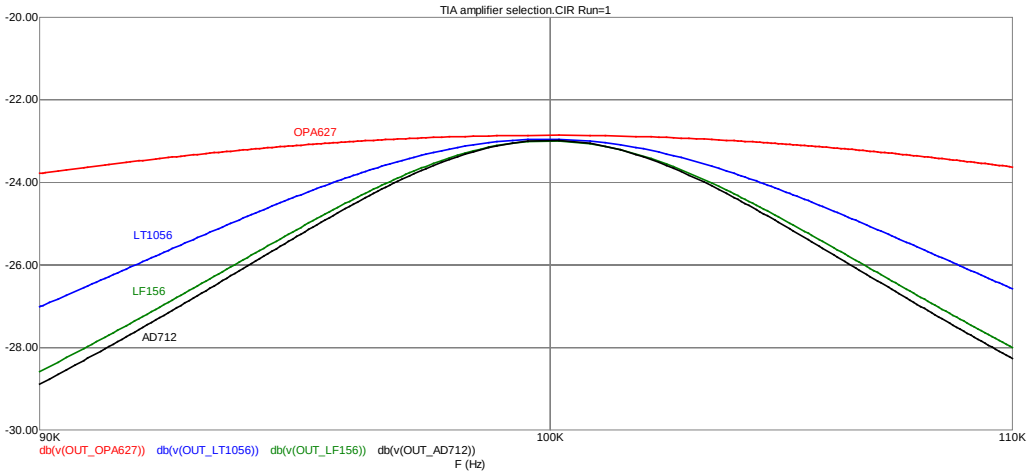

Figure 2-30 The transfer function for OPA627 (red), LT1056 (blue), LF156 (green) and AD712 (black) amplifiers (TIA) for the 100 kHz ± 10 kHz frequency range. The gain at 100 kHz is around -23 dB for ΔC = 0,12 pF

The best amplifier, the OPA627, is not a space-qualified part, but it is available in the MIL temperature range. The LT1056 exists as the RH1056 space-qualified part version and the remaining two (LF156 and AD712) have some space heritage. The gain bandwidth product of the above amplifiers is 16 MHz, 6,5 MHz, 5 MHz and 4 MHz, respectively. Therefore, the best space FET TIA, currently only evaluated with respect to the gain flatness, would be RH1056. Characteristics of candidate amplifiers suitable for the TIA application are compared in Table 2-27.

Table 2-27 Operational amplifiers suitable for TIA application. All parts are FET amplifiers, except the bipolar OP467, a space-qualified type, which would require discrete FET input due to its large current noise

Part number	Manufacturer	Voltage noise at 1 kHz	Current noise at 1 kHz	Slew rate	Gain bandwidth	Power (±7.5 V)
RH1056A / LT1056	Linear Technology	$14\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$1{,}8\,\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$	$16\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	6,5 MHz	75 mW
LF156	National	$12\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$10\,\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$	$12\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	5 MHz	75 mW
AD712	Analog Devices	$18\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$10\,\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$	$20\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	4 MHz	75 mW
OPA627	Texas Instruments	$5{,}2\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$1{,}6\,\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$	$55\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	16 MHz	105 mW
OP467S / OP467	Analog Devices	$6\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	$800\,\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$	$125\,\frac{\mathrm{V}}{\mu\mathrm{s}}$	28 MHz	120 mW

Unfortunately, all space parts have a larger voltage noise than the military part OPA627. Because of large amplifier feedback impedance, the current noise shall be in $fA/\sqrt{Hz}$ range, this being the reason why only FET input amplifiers can be used. This will be further analyzed during TIA modeling in 2.8.4. The last part in the table, also the space-qualified part, is a good solution for the main amplifier but could be used for TIA if buffered by some low-noise discrete FET stage.

2.8.3 TIA Transfer Function

The analytical model of the differential TIA transfer function is derived in APPENDIX B.

It is noted during the evaluation that the transfer function (B-11) is too complex for use and therefore, it needs simplification for the circuit design. Much like in the case of the simple model (2.18), the sensing bridge output U_{BR} is a product of the bridge impedance Z_{BR}, the TM injection voltage U_M, the differential capacitance being measured ΔC and $s = j\omega$. In the detailed model (B-15) there are also attenuation factors due to the transformer primary to secondary coupling K and the actuation and bridge tuning capacitors C_a and C_p, respectively.

$$U_{BR}(s) = K\frac{C_\mathrm{a}}{C_\mathrm{a} + C_p} \cdot s \cdot Z_{BR} \cdot U_M \cdot \Delta C \tag{2.89}$$

The simplified TIA transfer function is derived under the assumption of an ideal op-amp with zero input capacitance (Figure B-1) and an infinite open loop gain, i.e., $C_{IN} = 0$ and $A = \infty$, respectively. Therefore, the transfer function of the ideal TIA can be written as

$$G_{TIA\_id}(s) = \frac{U_O}{U_{BR}} = \frac{Z_{FB}C_D s + 1}{\frac{Z_{BR}C_D}{2}s + 1} \tag{2.90}$$

where U_O is the TIA output, Z_{FB} is the TIA feedback impedance, C_D the TIA decoupling capacitor and the coefficients of the denominator in (B-11) simplify to $\alpha = 0$ and $\beta = Z_{BR}C_D/2$.

To simplify, the decoupling capacitor C_D (Figure B-1) can be neglected, i.e., $C_D = \infty$ (zero impedance for 100 kHz). Furthermore, the feedback impedance Z_{FB} is approximately the impedance of the capacitor C_{FB} at 100 kHz, i.e., $|Z_{FB}| = 481{,}7\,\mathrm{k\Omega}$ and $1/\omega C_{FB} = 482{,}3\,\mathrm{k\Omega}$, respectively. With these simplifications, the simple TIA transfer function (index S) can be written as

$$G_{TIA\_S}(\omega) = \frac{2}{|Z_{BR}|\omega C_{FB}} = \frac{2}{R_{BR}\omega C_{FB}} \tag{2.91}$$

where the bridge impedance takes a real value R_{BR} at resonant frequency.

The TIA output is calculated by multiplying the bridge output by the TIA transfer function and therefore, the simplified TIA output is calculated from (2.89) and (2.91).

$$U_{O\_S} = U_{BR}(\omega) \cdot G_{TIA\_S}(\omega) = K\frac{C_{\mathrm{a}}}{C_{\mathrm{a}} + C_p} \cdot \frac{2\Delta C}{C_{FB}} \cdot U_M \tag{2.92}$$

The attenuation factor $K\,C_{\mathrm{a}}/(C_{\mathrm{a}} + C_p)$ in the exemplary design, given by Table B-1, is approximately 0,92. Assuming that this factor is relatively constant, the sensing gain is defined by a single parameter, the feedback capacitor C_{FB}, which is the most important advantage of the TIA circuit. Since the gain must be maximized at the front stage, the smallest capacitor C_{FB} = 3,3 pF is selected. The smallest space qualified capacitor is 10 pF, which requires a series combination to achieve smaller values. On the other hand, larger values of feedback capacitors reduce gain and cause a flatter TIA transfer function around 100 kHz.

With the parameters given in Table B-1, the approximated TIA output calculated by (2.92) will be 40,15 mV, which is very close to the output of the detailed model of 39,8 mV (Figure B-4).

2.8.4 TIA Noise Model

The noise calculation of an operational amplifier is described in many references, e.g., in [46]. The TIA noise sources and the noise gain (*NG*) of the amplifier are analytically derived in APPENDIX C.

The voltage noise spectral densities at the TIA output are amplified by the sensing gain, which is in this analysis simplified to unity since it does not change the SNR. In addition, the demodulation process amplifies the noise by factor $\sqrt{2}$, as already mentioned in 2.1.2 and explained in 2.10.

The TIA voltage noise sources at the sensing output are summarized below:

$$e_{TH-ZBR} = \sqrt{2} \cdot \sqrt{4k_B T \Re[Z_{BR}]} \cdot G_{TIA}$$

$$\Re[Z_{BR}] = \frac{R_L}{1 - \omega^2 K \frac{C_a}{C_a + C_p'} LC_{eq}' \left\{2 - \omega^2 K \frac{C_a}{C_a + C_p'} LC_{eq}' \left[1 + \left(\frac{R_L}{\omega L}\right)^2\right]\right\}} \tag{2.93}$$

where $e_{TH\text{-}ZBR}$ is the thermal noise of the real part of the sensing bridge impedance $\Re[Z_{FB}]$, G_{TIA} is the TIA differential signal gain (transfer function) defined by (B-11) and factor $\sqrt{2}$ is due to the demodulation process. The remaining parameters of the bridge are explained in APPENDIX C, with exemplary values given in Table B-1.

$$e_{TH-ZFB} = 2 \cdot \sqrt{4k_B T \Re[Z_{FB}]} \tag{2.94}$$

where $e_{TH\text{-}ZFB}$ is the thermal noise of the real part of the TIA feedback impedance $\Re[Z_{FB}]$, defined by (C-4), and factor 2 is due to the differential TIA and the demodulation process.

$$e_{i-AMP} = 2 \cdot i_{AMP} \cdot |Z_{FB}| \tag{2.95}$$

where $e_{i\text{-}AMP}$ is the equivalent voltage noise resulting from the amplifier current noise i_{AMP} flowing through the TIA feedback impedance $|Z_{FB}|$. The $|Z_{FB}|$ is defined by (C-5) and factor 2 is due to the differential TIA and the demodulation process.

$$e_{u-AMP} = 2 \cdot u_{AMP} \cdot NG \tag{2.96}$$

where $e_{u\text{-}AMP}$ is the TIA voltage noise, the noise gain *NG* is defined by (C-8) and factor 2 is due to the differential TIA and the demodulation process.

The plot of all four noise sources calculated by the above equations and using the sensing front-end parameters given in Table B-1 is shown in Figure 2-31. As already mentioned, the voltage levels assume a unity sensing gain after the TIA and a unity gain of the demodulator.

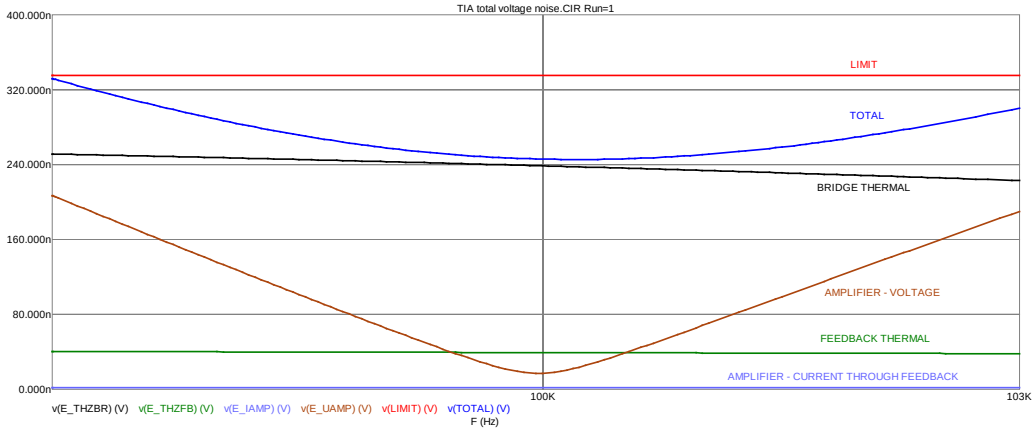

Figure 2-31 Comparison of the sensing noise sources against the sensing limit in the frequency range of 100 kHz ± 3 kHz and the amplitude range of 400 $nV/\sqrt{Hz}$

As previously stated, the dominating noise source is the thermal noise of the sensing bridge, which depends on the bridge quality factor *Q*. The voltage noise limit at the sensing output is calculated from the capacitance noise limit given in Table 2-7 and the conversion factor at the TIA output $|\partial U_O/\partial \Delta C|$, which is calculated by differentiating (2.92).

$$S_u^{1/2} = S_{\Delta C}^{1/2} \left|\frac{\partial U_O}{\partial \Delta C}\right| = 1 \frac{aF}{\sqrt{Hz}} \cdot K \frac{C_a}{C_a + C_p'} \frac{2U_M}{C_{FB}} = 335 \frac{nV}{\sqrt{Hz}} \tag{2.97}$$

With the minimum *Q* of 200 the sensing noise is equal to 73% of the limit or 246 $nV/\sqrt{Hz}$.

2.8.5 AC Amplifier

The main amplifier shown in Figure 2-32 is a standard AC amplifier circuit with the high-pass filter time constant ($R_{IN} \cdot C_{IN}$) and a corresponding corner frequency substantially below the sensing carrier frequency of 100 kHz so as not to influence the signal phase. Therefore, the corner frequency around 10 kHz is suggested.

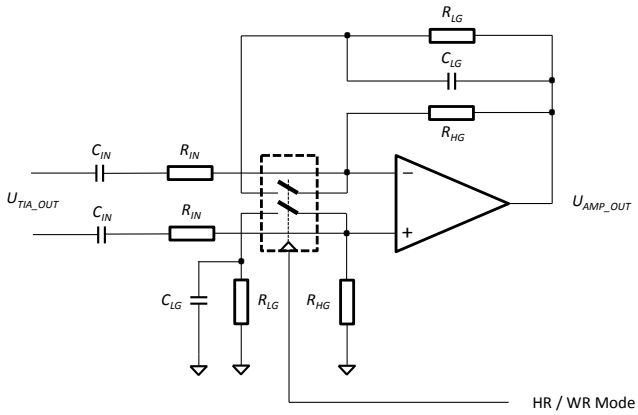

Figure 2-32 The main sensing amplifier with the gain switching for the High Resolution (HR) mode and the Wide Range (WR) mode with corresponding high and low gain circuit elements

The voltage per capacitance gain $|\partial U_{BR}/\partial \Delta C|$ is, according to (2.97), approximately 0,33 V/pF at the TIA output. In the HR mode with the ±0,12 pF measurement range, the TIA is generating the sinusoidal signal with 39,6 mV amplitude. Assuming the total voltage dynamic range to be ±1,8 V in the AC sensing path, the amplifier will have the gain G_{HG} = 45,4. In the WR mode the capacitance range is ±2,5 pF and the TIA output of ±825 mV is expected. Therefore, the amplifier gain in this mode will be 2,5 / 0,12 = 20,83 times smaller or G_{LG} = 2,18. Since at the low gain the amplifier has larger bandwidth, some filtering is added in the feedback path (C_{LG}) to reduce gain peaking.

Since in this application the input impedance is low (TIA output), a bipolar type, low voltage noise op-amp can be used like the space-qualified OP467 with characteristics provided in Table 2-15. The commercial part with the lowest noise in this class is the AD797 with the $0{,}9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ noise. Note that it is not necessary to find an amplifier with extremely low noise because the sensing bridge noise is at the level of approximately $240\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (Figure 2-31). The space-qualified quad analog switch HS1-302RH is an adequate part for the gain switching application. Even though this is a high-speed part that can be used for the demodulator circuit, the speed is not the main requirement here. Nevertheless, reducing the number of different parts on the schematic is beneficial. The commercial dual analog switch MAX321 is a suitable part for prototyping.

2.9 Band-Pass Filter

Both the band-pass filter and the demodulator perform a similar function, the extraction of the signal at 100 kHz from the noise. By removing some of the out-of-band noise, the band-pass filter will thus improve the performance of the demodulator. One possible filter solution is shown in Figure 2-33.

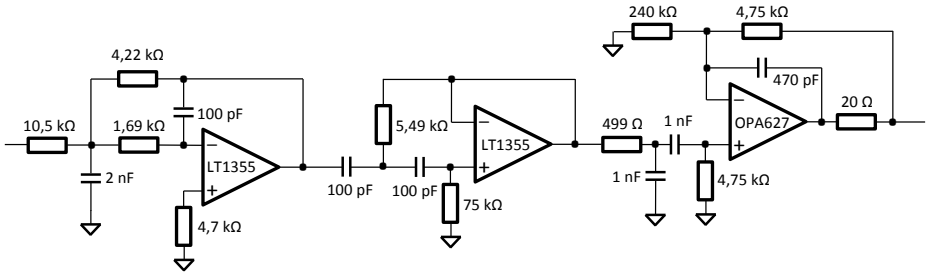

Figure 2-33 The third order active / passive band-pass filter and the demodulator driver

The composite filter circuit consists of a second-order, active low-pass filter (first op-amp), a high-pass filter (second op-amp) and a first order band-pass passive filter. The passive filter is buffered by the amplifier OPA627, providing the adjustment of the total filter gain and the drive capability for the capacitive load of the demodulator.

Since the analog demodulator is not ideal, large out-of-band noise could leak into the demodulated band. Therefore, with a narrower band-pass filter the demodulator will have an "easier" task. On the other hand, the gain of a filter with a very narrow pass-band is more sensitive to the fluctuation of its components (resistors and capacitors) with temperature.

Moreover, as these filters require very under-damped transfer functions, the op-amp selection with respect to the open-loop gain and the slew rate becomes very critical. As an example, for the high-pass filter corner frequency of 90 kHz, i.e., a very narrow pass-band filter, the required damping factor ξ must be 0,1 to achieve a flat pass-band. Such a low damping factor means a five times larger gain close to the corner frequency. On the other hand, for a filter

with a larger pass-band, e.g., with the high-pass filter corner frequency of 70 kHz, the necessary damping factor ξ = 0,32, which means only a 66% larger gain.

The parameters of the band-pass filter shown in Figure 2-33 (schematic) and Figure 2-34 (transfer function) are summarized in Table 2-28.

Table 2-28 Parameters of the third order band-pass filter

	DC, AC Gain	Gain at 100 kHz	Corner frequency	Damping factor ξ	Lower -3 dB frequency	Higher -3 dB frequency
2nd order low-pass	0,402	1,7	133,3 kHz	0,276	70,9 kHz	140,4 kHz
2nd order high-pass	1	0,7	78,4 kHz	0,271		
1st order band-pass	0,82	0,82	-	-	25,8 kHz	408,5 kHz
Output driver	1,02	1,02	-	-	-	9,6 MHz
Combined filter	-	1	-	-	71,4 kHz	139,5 kHz

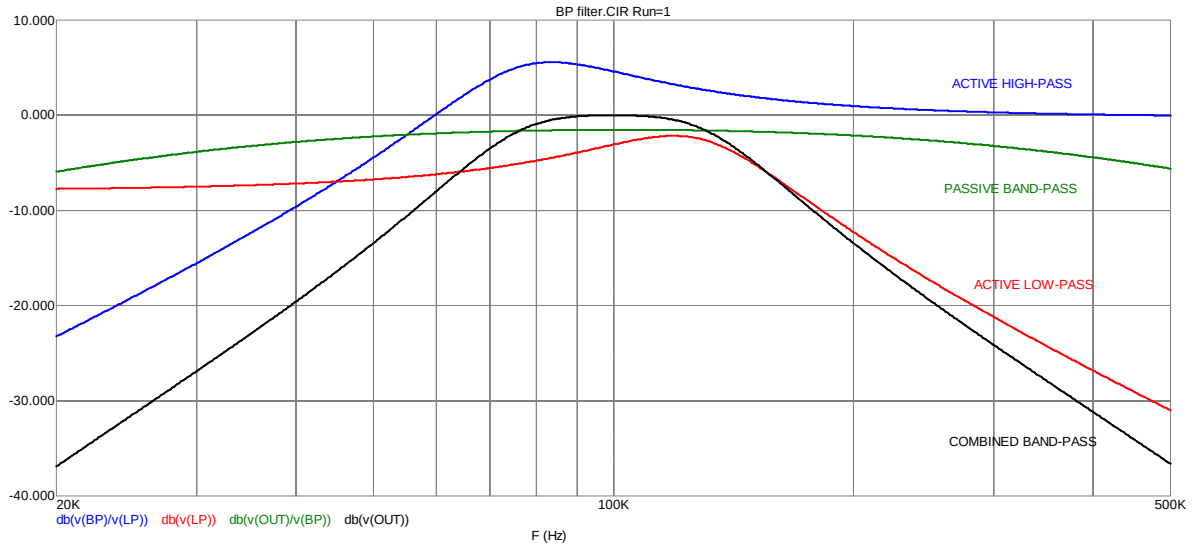

Figure 2-34 Transfer functions of each filter stage in the frequency band from 20 kHz to 500 kHz and the magnitude from -40 dB to 10 dB

2.10 Synchronous Demodulator

The signal exiting the band-pass filter has a 100 kHz carrier, which is modulated such that the amplitude represents the TM position from the center of its enclosure. For the TM movement at the low frequency *f*, the Fourier transform of a modulated signal has two sidebands, one above and one below the carrier frequency f_c, i.e., $f_c + f$ and $f_c - f$, respectively. This is known as the double-sideband amplitude modulation (DSB-AM) process. Because of the two sidebands, the bandwidth of a modulated signal is twice as wide compared with the bandwidth of the non-modulated signal.

In the demodulation process the carrier frequency is removed by multiplying (mixing) the modulated signal $A(t)cos(\omega_0 t)$ with the same carrier signal $cos(\omega_0 t)$ used for modulation and then by low-pass filtering of the product. The phase of the carrier signal used in the

demodulation process is properly tuned to maximize the in-phase signal. Equal frequency and the proper phase of the demodulation control signal hence give rise to other used names for this process, such as phase synchronous demodulation or the lock-in technique.

The demodulation process will also reduce the amplitude signal *A(t)* by a factor of two, which can be easily shown with trigonometric equations. Since the additional gain in the sensing circuit will not affect the signal-to-noise ratio (SNR), the gain can be assumed in this analysis to be one. To compensate for the factor two signal loss, the multiplication can be performed with a signal twice as large, i.e., $2cos(\omega_0 t)$. It is of interest in this simple analysis to determine whether the noise is equal before and after the demodulation process. The noise after the band-pass filter, i.e., before the demodulator, can be represented by its in-phase and in-quadrature component, each having equal power density

$$\begin{gathered} n(t) = n_c(t)cos(\omega_0 t) - n_s(t)sin(\omega_0 t) \\ S_{n_c}(\omega_0) = S_{n_s}(\omega_0) = \frac{N_0}{2} \end{gathered} \tag{2.98}$$

where N_0 is the noise amplitude and "c" and "s" subscripts indicate cosine (in-phase) and sine (in-quadrature) components. The (input) noise power of the modulated signal is the integral of the noise power density in the whole bandwidth, which can be written as

$$N_{in} = \langle n^2(t) \rangle = 2\int_0^\infty S_n(f)df = 2\int_{f_0-W}^{f_0+W} \frac{N_0}{2} df = 2N_0 W \tag{2.99}$$

where W is the bandwidth of each sideband of the modulated signal.

The demodulation process with $2cos(\omega_0 t)$ can be written as

$$\begin{gathered} n_{LP}(t) = [n(t) \cdot 2cos(\omega_0 t)]_{LP} \\ n_{LP}(t) = [2n_c(t)cos^2(\omega_0 t) - 2n_s(t)cos(\omega_0 t) \cdot sin(\omega_0 t)]_{LP} \\ n_{LP}(t) = [n_c(t) + n_c(t)cos(2\omega_0 t) - n_s(t)sin(2\omega_0 t)]_{LP} = n_c(t) \end{gathered} \tag{2.100}$$

where $[\ldots]_{LP}$ means low-pass filtering with the filter corner frequency $\omega_{LP} << \omega_0$. Therefore, the noise components at twice the carrier frequency are removed by filtering. Since from (2.100) the demodulated noise remains equal to the input modulated noise, its power also remains equal, as indicated below.

$$N_{out} = \langle n_{LP}^2(t) \rangle = \langle n_c^2(t) \rangle = 2N_0 W = N_{in} \tag{2.101}$$

In the demodulation process with the low-pass filtering at the end, the bandwidth of the output signal is twice smaller than the bandwidth of the modulated signal. Since power density is calculated by dividing the power by the bandwidth, the input and output noise densities will not be the same. With equal input and output noise power and a twice smaller bandwidth at the output, the conclusion is that the noise density is twice larger after the demodulation.

$$S_{n_{LP}}(\omega_{LP}) = N_0 = 2S_{n_c}(\omega_0) \tag{2.102}$$

The factor 2 in the power spectral density (PSD) is already included in the analyses presented in 2.1.2 and 2.8.4. For the amplitude spectral density (ASD), this factor is therefore $\sqrt{2}$.

2.10.1 Demodulation Circuit

An example of the demodulator circuit is shown in Figure 2-35. Its purpose is to extract the 100 kHz signal from the noise and convert the signal amplitude into the DC voltage. Note that the noise can be larger than the signal.

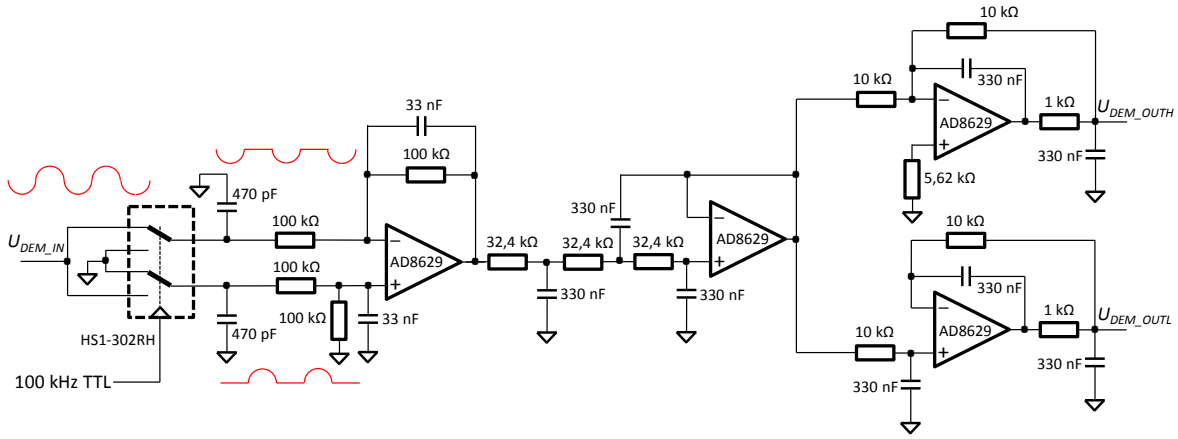

Figure 2-35 The demodulator circuit with the low-pass filters and the ADC drivers

To separate the signal from the noise, the demodulator locks to the signal frequency using the proper control signal and averages other (noise) frequencies to zero. To average the AC signal to a DC voltage, the signal is first rectified using an analog switch. This rectification has the same function as the mixing (multiplication) of two frequencies in the standard amplitude demodulation process. With the control signal exactly in phase with the input signal, the analog switch is inverting the signal exactly when it is changing the phase so that the first differential amplifier in Figure 2-35 can always provide the same signal sign on its output. Since the noise is randomly changing the phase with respect to the demodulator control signal, it is not properly rectified and is therefore averaged to zero.

To attenuate the switching spikes due to the charge injection, an unavoidable process in every analog switch, the switch is loaded with the 470 pF capacitors. While the spike level goes down with this capacitance, its duration increases. The space-qualified analog switch HS1-302RH from Intersil with the turn ON/OFF time (T_{ON}, T_{OFF}) of 300 ns and the faster 50ns ADG201HS analog switch from Analog Devices, already listed in Table 2-10, are suggested for this function. For prototyping, their commercial equivalents or MAX391_2_3 can be used.

In absence of post filtering, a full wave rectified signal would appear at the demodulator output. The conversion from the signal peak level to the averaged DC level in the low-pass filtering involves an attenuation factor of $2/\pi$. Once the signal is in the DC domain, the low frequency drifts in op-amps can greatly affect the sensing performance. Therefore, all op-amps in the chain are suggested to be zero-drift or auto-zero amplifiers, which do not exhibit the 1/f noise. The space qualified AD8629 amplifier with characteristics already given in Table 2-13 is a suitable part because of rail-to-rail input / output characteristics and low noise. The alternative space part, the LMP2012, provides limited rail-to-rail feature, i.e., only on output, and not on input, and thus is limiting maximum input common voltage level. Both parts can support a maximum ±2,5 V bipolar power supply or unipolar +5 V.

Since the AC circuits before the demodulator have the full-scale range of ±1,8 V, the attenuation factor $2/\pi$ will set the demodulator full-scale DC output to ±1,146 V. The AD8629 has internal auto-zero switching at about 15 kHz, which can alias with the 200 kHz ripple signal of the demodulator and fall into the signal low frequency band. The ripple shall

therefore be reduced to eliminate aliasing. The first stage filtering corner frequency is set to 48 Hz to reduce the 200 kHz averaging ripple to less than one mV at the maximum input signal level.

The second stage is a third order, unity gain Sallen-Key low-pass filter with the Butterworth response at the -3dB corner frequency of 5 Hz. The last stage consists of the non-inverting and inverting auto-zero buffers, each including low-pass filtering to remove the auto-zero switching noise. These buffers double the demodulator output (±2,292 V) and provide some signal margin to the ADC full-scale differential input of ±2,5 V.

2.11 Analog to Digital Conversion

The ADC is the last element in the sensing chain. The part itself and the digital data processing shall be selected so as to generate negligible quantization noise compared with the input analog noise.

For the ±2,5 V ADC full-scale range, the equivalent capacitance range can be set to ±0,131 pF in the HR mode and ±2,728 pF in the WR mode. This selection provides some margin for the minimum measurement range of ±0,12 pF and ±2,5 pF, respectively and a rounded number of aF for the ADC least significant bit (LSB) size.

Currently there are no space qualified A/D converters with more than 16-bit resolution. The suggested 16-bit ADC with a space heritage is LTC1604 from Linear Technology [47]. This is the high-speed sampling type ADC with the signal to noise and distortion ratio SINAD = 90 dB. It can be shown that the quantization noise of this ADC is twice the sensing noise limit if only one range is implemented and therefore, a gain switching (HR and WR mode) must be implemented. The effective number of bits (ENOB) can be calculated from the SINAD by

$$ENOB = \frac{SINAD - 1{,}76\ dB}{6{,}02} = 14{,}66 \tag{2.103}$$

and the ADC quantization noise in HR mode is therefore,

$$e_{q\_ADC\_HR} = \frac{LSB_{eff}}{\sqrt{12 f_N}} = \frac{2 \cdot 0{,}131\ pF}{2^{ENOB}\sqrt{12 \cdot 640\ Hz}} = 0{,}115\ \frac{aF}{\sqrt{Hz}} \tag{2.104}$$

where f_N is the Nyquist frequency and $2f_N$ is the ADC sampling frequency. The LSB size of the 16-bit ADC, for the selected HR range of ±0,131 pF, is LSB_{ADC} = 4 aF and the effective LSB size, due to the ADC ENOB, is LSB_{eff} = 10,1 aF. The ADC output at the selected sampling frequency of 1280 Hz must be further averaged and decimated 128 times to achieve the final data rate of 10 Hz. With the averaging ratio R = 128, the LSB_{ADC} size is reduced 128 times and the number of bits is enlarged by 7 bits, i.e., to LSB_{OUT} = 0,03125 aF and N = 23, respectively.

Assuming that the ADC quantization noise is a white noise, the noise is reduced by factor $\sqrt{R}$ after averaging. With the moving average algorithm, the output data rate remains 1280 Hz and therefore must be decimated (by removing 127 samples) to the output data rate of 10 Hz. The decimation process enlarges the quantization noise by factor $\sqrt{R}$, which can be easily confirmed by (2.104). Therefore, the output noise after averaging and decimation remains the same, i.e., $0{,}115\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$. This is about 10 times smaller than the sensing noise limit of $1\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ (Figure 2-12), from which it can be concluded that the ADC quantization noise is negligible. For the selected ADC HR full-scale range, the sensing output sensitivity is 32 LSB/aF.

The LSB size of the 16-bit ADC for the selected range of ±2,728 pF in the WR mode is LSB_{ADC} = 83,25 aF and the effective LSB size, due to the ADC ENOB, is LSB_{eff} = 210,75 aF. After averaging and decimation, the LSB_{OUT} = 0,65 aF and the quantization noise is $2{,}4\ \mathrm{aF}/\sqrt{\mathrm{Hz}}$.

$$e_{q\_ADC\_WR} = \frac{LSB_{eff}}{\sqrt{12 f_N}} = \frac{2 \cdot 2{,}728\ pF}{2^{ENOB}\sqrt{12 \cdot 640\ Hz}} = 2{,}4\ \frac{aF}{\sqrt{Hz}} \tag{2.105}$$

This is roughly 6 times smaller than the sensing noise limit of $15\ \mathrm{aF}/\sqrt{\mathrm{Hz}}$ (Figure 2-13). For the selected ADC WR full-scale range, the sensing output sensitivity is 1,538 LSB/aF or 20,8 times smaller than in the HR mode.

The ADC voltage reference noise analyzed in 2.5.2, with its $30\ \mathrm{ppm}/\sqrt{\mathrm{Hz}}$ design limit, is also negligible compared with the sensing noise limit. Therefore, this analysis shows that the 16-bit ADC can be used, but the whole signal dynamic range must be divided into two ranges associated to the initial TM stabilization/centering operation after its release (WR mode) and the science operations (HR mode).

Chapter 3
ELECTROSTATIC ACTUATION OF TEST MASS

On the LISA and LPF missions the S/C will slowly drift against the free falling TM due to the striking particles coming from the sun (the solar wind) or from outer space. The micro-Newton thrusters on S/C will compensate this drift, but not in all degrees of freedom (DOFs) and definitely not against both TMs located inside the S/C. Therefore, electrostatic actuation must be used on those DOFs that are not controlled by the S/C thrusters to correct the position of the TM against the S/C. Despite the gravitational tuning with small masses, the gravitational imbalance in the S/C will not be negligible and will affect the TMs. The electrostatic actuation shall therefore have enough authority (strength) to compensate this imbalance on all the axes. Since the actuation also introduces the stray acceleration (force) noise, it will not be used on the main *x*-axis in line with the laser beam (Figure 2-2), but will be used, e.g., to correct TM rotation φ around the *z*-axis.

The same 12 sensing electrodes around the TM are used for the actuation purpose. Voltages applied on electrodes either on front / rear side of the TM or on corners (Figure 3-1) generate electrostatic forces that control the TM in translation or rotation, respectively.

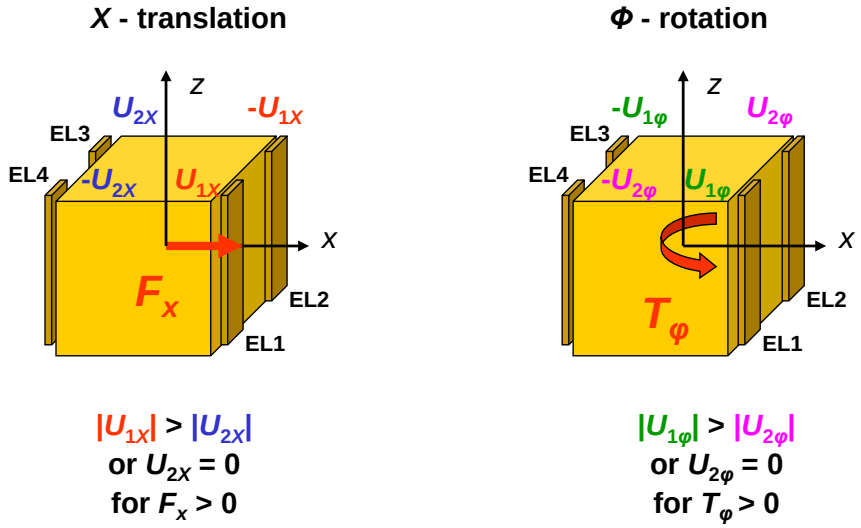

Figure 3-1 Actuation principle in x-φ DOFs: actuation voltages U_{1x} and U_{2x} applied on the TM face electrodes generate differential force F_x to control the TM in translation, while voltages $U_{1\varphi}$ and $U_{2\varphi}$ applied on the TM corner electrodes generate differential torque T_φ to control the TM in rotation. Since electrostatic force/torque is proportional to the square of the voltage, both positive and negative voltages have the same effect

3.1 Main Actuation Requirements

Top science requirements, from which the TM actuation requirements can be derived, have their origin in the residual TM stray acceleration limited by (2.51) and (2.52) for LISA and LTP, respectively. Note that the (2.51) LISA requirement is given only for the sensitive *x*-axis. All other axes in LISA must satisfy the 10 times relaxed LTP requirement (2.52). The ten times relaxed requirement for LTP is used to derive the actuation acceleration noise limits, which are then also applicable to LISA. This is acceptable because electrostatic actuation is not used for the most sensitive (drag-free) *x*-axis in LISA and the cross coupling requirements from other DOFs to the *x*-axis "attenuate" the LTP actuation noise levels enough to satisfy the more stringent LISA noise level for the sensitive *x*-axis.

The total LTP stray acceleration noise budget of $30\ \mathrm{fms^{-2}/\sqrt{Hz}}$ (2.52) is dominated by the TM actuation noise [26] generated by FEE and is limited to

$$S_{a_{ACT}}^{1/2} \leq 10\ \frac{fm}{s^2\sqrt{Hz}} \tag{3.1}$$

The stiffness between the S/C and the TM is also generating stray acceleration by coupling with the residual jitter between the TM and the S/C. The maximum TM to S/C jitter in LISA is $2{,}5\ \mathrm{nm/\sqrt{Hz}}$ on the *x*-axis and $10\ \mathrm{nm/\sqrt{Hz}}$ on the *y*, *z*-axes [26]. The jitter multiplies with the stiffness of $3 \times 10^{-7}\mathrm{s^{-2}}$ [26], resulting in a stray acceleration of $0{,}75\ \mathrm{fms^{-2}/\sqrt{Hz}}$ on the drag-free *x*-axis and $3\ \mathrm{fms^{-2}/\sqrt{Hz}}$ on the other axes. These stray accelerations are negligible compared with the *x*-axis and the *y*-, *z*-axes requirements of $3\ \mathrm{fms^{-2}/\sqrt{Hz}}$ and $30\ \mathrm{fms^{-2}/\sqrt{Hz}}$, respectively. Other sources of noise, entering in (2.52), are not of FEE origin and are therefore not analyzed here.

The requirement (3.1) breaks down into several requirements for acceleration noise [48], which shall be converted into the electrical requirements of the actuation circuits. The actuation voltages are AC waveforms with frequencies in the audio band, selected not to mix with the sensing 100 kHz frequency[8]. An assessment of options and a selection of actuation waveforms is given in 3.1.5, but for this analysis the frequency band of actuation frequencies is assumed to be between 60 Hz and 270 Hz.

The most important actuation noise source is the multiplicative noise in the measurement bandwidth (MBW) due to actuation amplitude stability. It is analyzed in 3.1.1 and is by [48] limited to

$$S_{a\_act\_amp}^{1/2} \leq 4{,}5\ \frac{fm}{s^2\sqrt{Hz}} \tag{3.2}$$

The additive voltage noise at AC actuation frequencies down-converts into MBW and generates stray acceleration on the TM. This noise is analyzed in 3.1.2 and limited by [48] to

$$S_{a\_act\_AC}^{1/2} \leq 2{,}8\ \frac{fm}{s^2\sqrt{Hz}} \tag{3.3}$$

The additive voltage noise in MBW due to the actuation DC noise is analyzed in 3.1.3 and limited in [48] to

$$S_{a\_act\_DC}^{1/2} \leq 0{,}36\ \frac{fm}{s^2\sqrt{Hz}} \tag{3.4}$$

To secure performance, [48] suggests a considerable acceleration noise margin of $8{,}5\ \mathrm{fms^{-2}/\sqrt{Hz}}$. The square root of the quadratic sum of (3.2), (3.3), (3.4) and the margin is then equal to (3.1).

3.1.1 Actuation Stability

The amplitude stability requirement of the actuation voltage is derived under the assumption of correlated multiplicative voltage noise of equal magnitude on all four actuations channels, assigned to the one quadruple of electrodes, and the worst-case (maximum) actuation forces/torques [49]. This means that actuation amplitude stability is governed by the DC stability of the common voltage reference used by four DACs which generate the AC actuation waveforms for the quadruple of electrodes. For this assumption, actuation acceleration noise is directly proportional to actuation amplitude stability and the level of

[8] Note that the same electrodes are used for sensing and actuation; thus, a frequency separation is needed.

applied acceleration on the TM, i.e., it is multiplicative.

$$S_{a\_act\_amp}^{1/2} = 2 \cdot a_0 \cdot S_{\Delta U/U}^{1/2} \tag{3.5}$$

Since the TM acceleration is proportional to the square of actuation voltage, i.e., $a \propto U^2$, the fluctuation (the differential) of the acceleration will be proportional to $2U \cdot \delta U = 2a\,\delta U/U$, which, by analogy, also applies to the noise in (3.5). The maximum *x*-axis acceleration authority in LTP required to compensate the local (S/C) gravitational field felt by two TMs is $a_0 = 1{,}3$ nm/s² [26]. With this acceleration authority and the acceleration noise limit (3.2), the relative amplitude stability of the voltage reference and thus the actuation amplitude will be limited to

$$S_{\Delta U/U}^{1/2} = \frac{S_{a\_act\_amp}^{1/2}}{2 \cdot a_0} = 1{,}73\,\frac{ppm}{\sqrt{Hz}} \approx 2\,\frac{ppm}{\sqrt{Hz}} \tag{3.6}$$

which is a very stringent requirement for electronics, especially because it must be satisfied at 0,1 mHz, where the 1/*f* electronics noise, the so-called pink noise, is inevitable.

3.1.2 Actuation AC Noise

The actuation AC noise refers to the additive voltage noise at the waveform frequency, which has been derived under the assumption of uncorrelated additive noise with equal magnitude on all four actuation outputs (electrodes) of one pair of DOFs (e.g., *x*-*φ*, Figure 3-1) and the worst-case (maximum) actuation forces/torques. This noise is down-converted by the AC waveform frequencies into the MBW due to amplitude modulation. It is analyzed in detail in [48] and can be written as

$$S_{a_x\_act\_AC}^{1/2} = \frac{\sqrt{2}}{m}\sqrt{\frac{\partial C_{ET}}{\partial x} - \frac{\partial C_{EH}}{\partial x}}\sqrt{F_{x\_max} + 2\,\frac{T_{\varphi\_max}}{R_\varphi}}\,S_{u\_AC}^{1/2} \tag{3.7}$$

where m is TM mass, $\partial C_{ET}/\partial x$ is the 1st order electrode to TM (ET) capacitance derivative, $\partial C_{EH}/\partial x$ is the 1st order electrode to housing (EH) capacitance derivative, F_{x_max} and T_{φ_max} are the maximum force and torque, R_φ is *φ*-torque lever arm (half a distance between electrodes on one TM face) and $S_{u\_AC}^{1/2}$ is the actuation AC voltage noise at the waveform frequency. With the values of these parameters specified in Table 3-1, with (3.7) and the acceleration noise limit (3.3), the requirement for the actuation AC voltage noise is

$$S_{u\_AC}^{1/2} = \frac{S_{a_x\_act\_AC}^{1/2}}{7{,}19 \times 10^{-10}} = 3{,}9\,\frac{\mu V}{\sqrt{Hz}} \approx 4\,\frac{\mu V}{\sqrt{Hz}} \tag{3.8}$$

3.1.3 Actuation DC Noise

The DC actuation noise beats (multiplies) with the residual DC stray voltages [24], [25] and accumulated charge on the TM, generating stray accelerations as indicated by (2.40) for any two voltages. The stray acceleration on the *x*-axis $S_{a_x\_act\_DC}^{1/2}$ due to these sources can be written according to [48] as

$$S_{a_x\_act\_DC}^{1/2} = \sqrt{2}\,\frac{2}{m}\left[\frac{\partial C_{ET}}{\partial x}\left(\frac{\Delta u_x}{2} + \frac{q_e q_0}{C_{tot}}\right) - \frac{\partial C_{EH}}{\partial x}\frac{\Delta u_x}{2}\right]S_{u\_DC}^{1/2} \tag{3.9}$$

where Δu_x is the average electrode stray DC voltage imbalance (between electrodes or any electrode and the TM), q_e is the electron charge, q_0 is the number of electron charges accumulated on the TM before being discharged, C_{tot} is the total TM capacitance to ground, $S_{u\_DC}^{1/2}$ is the actuation DC voltage noise and other parameters have been explained earlier.

With the values of these parameters specified in Table 3-1, with (3.9) and the acceleration noise limit (3.4), the requirement for the actuation DC voltage noise is

$$S_{u\_DC}^{1/2} = \frac{S_{a_x\_act\_DC}^{1/2}}{3{,}81 \times 10^{-11}} = 9{,}45\,\frac{\mu V}{\sqrt{Hz}} \approx 10\,\frac{\mu V}{\sqrt{Hz}} \tag{3.10}$$

The requirement (3.10) must also be satisfied at 0,1 mHz, which makes it very challenging.

Table 3-1 Parameters involved in calculation of the TM stray acceleration

Parameter	Value	Note
TM mass	m = 1,96 kg	Design
Electrode to TM capacitance derivative (gradient)	$\frac{\partial C_{ET}}{\partial x} = 291{,}39\,\frac{\mathrm{pF}}{\mathrm{m}}$	Design
Electrode to housing capacitance derivative (gradient)	$\frac{\partial C_{EH}}{\partial x} = 69{,}67\,\frac{\mathrm{pF}}{\mathrm{m}}$	Design
Maximum *x*-force	$F_{x\_max} = 2{,}55$ nN	Requirement
Maximum φ-torque	$T_{\varphi\_max} = 10{,}37$ pNm	Requirement
φ-torque lever arm	R_φ = 10,75 mm	Design
Electrode stray voltage imbalance	$\Delta u_x = 0{,}115\ V$	Measured average value
Electron charge	$q_e = 1{,}6022 \times 10^{-19}$C	Constant
Accumulated number of charges	$q_0 = 1 \times 10^7$	Assumption
TM capacitance to ground	$C_{tot} = 34{,}2$ pF	Analysis

3.1.4 Actuation Range

Much like in sensing, the signal dynamic range in actuation is very large. This requires two modes of operation, namely HR and WR. Immediately after its release in the WR mode, the TM can have a high[9] velocity and the FEE will apply much larger actuation forces and torques to stabilize the TM for the science operation in HR mode. The minimum WR and HR mode acceleration levels for the LTP mission are given in Table 3-2 and Table 3-3, respectively [50]. The LISA actuation levels are smaller than in LTP because of different S/C configuration and expected better gravitational balancing.

Table 3-2 WR mode acceleration levels

DOF	*x*	*y*	*z*
Linear acceleration	$0{,}74\,\frac{\mu\mathrm{m}}{\mathrm{s}^2}$	$0{,}74\,\frac{\mu\mathrm{m}}{\mathrm{s}^2}$	$0{,}44\,\frac{\mu\mathrm{m}}{\mathrm{s}^2}$
DOF	φ	θ	η
Angular acceleration	$22{,}5\,\frac{\mu\mathrm{rad}}{\mathrm{s}^2}$	$31{,}2\,\frac{\mu\mathrm{rad}}{\mathrm{s}^2}$	$18{,}8\,\frac{\mu\mathrm{rad}}{\mathrm{s}^2}$

Table 3-3 HR mode acceleration levels

DOF	*x*	*y*	*z*
Linear acceleration	$1{,}3\,\frac{\mathrm{nm}}{\mathrm{s}^2}$	$2{,}2\,\frac{\mathrm{nm}}{\mathrm{s}^2}$	$3{,}7\,\frac{\mathrm{nm}}{\mathrm{s}^2}$
DOF	φ	θ	η
Angular acceleration	$16\,\frac{\mathrm{nrad}}{\mathrm{s}^2}$	$27\,\frac{\mathrm{nrad}}{\mathrm{s}^2}$	$23\,\frac{\mathrm{nrad}}{\mathrm{s}^2}$

[9] Maximum linear and angular velocities after the TM release are estimated to ±5 μm/s and ±100 μrad/s respectively [50], which are high compared to the science (HR) mode electrostatic actuation authority

Depending on the selected actuation scheme and the type of waveforms, actuation accelerations require different actuation voltages, which are assessed in the next section.

3.1.5 Actuation Waveforms

To solve the conversion laws for electrode voltage to force / torque, several constraints have been put in place [25], [51]:

- Voltages on electrodes must keep zero TM potential (in absence of TM charge)
- Voltages on electrodes must be orthogonal so that crosstalk between translational and rotational DOFs is avoided
- Voltages on electrodes shall be chosen to produce constant stiffness over the range of required forces (only in the HR, i.e., the science mode)

The first constraint requires that the sum of electrode voltages be zero, e.g., by applying $\pm U_j$ as indicated in Figure 3-1. The forces contributions would add up, as they depend on the square of the voltage drop between the TM and the electrodes and not their sign.

The second constraint can be accomplished by applying actuation voltages $U_x(t)$ and $U_\varphi(t)$ that have a *product* with zero average over time. Since x and φ voltages are applied on the same electrodes (Figure 3-1), the actuation voltages for each DOF must be either separated in time or in frequency. This will be further discussed in 3.3.1 and 3.3.2.

The electrode voltages produce acceleration on the TM and the parasitic coupling, i.e., the stiffness that is proportional to the level of acceleration. A control law can be designed, according to the third constraint, to maintain the resultant actuation stiffness over all electrodes constant for all forces. This can be accomplished by applying equal common voltage on four electrodes when zero forces and torques are needed and differential voltages to achieve the required differential forces or torques. The common voltage must in this scheme be equal to $U_{max}/\sqrt{2} \propto F_{max}/2$. For maximum force, the differential forces $\pm F_{max}/2$ would then be applied, which would require U_{max} voltage on one side of the TM and zero on the other. In both the zero and the maximum force cases, the stiffness would be equal, i.e., $2F_{max}/d$ [51], where d is the electrode gap against the TM in centered position.

3.2 Actuation Channel Architecture

The architecture of one actuation channel (12 in total for each TM) is suggested in Figure 3-2, which follows the conceptual design shown in Figure 2-2.

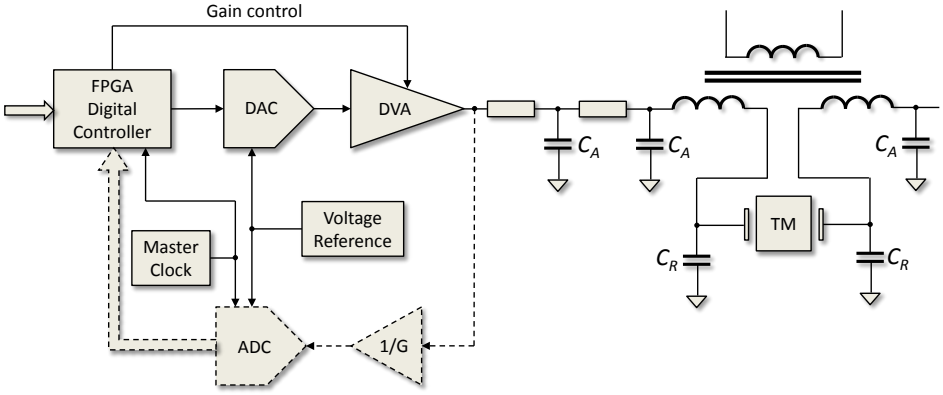

Figure 3-2 Architectural block diagram of one actuation channel with the D/A Converter (DAC), Drive Voltage Amplifier (DVA) and the low-pass filter. The feedback circuit with the attenuator and the A/D Converter (ADC) is used in an optional design with the Proportional, Integral and Derivative (PID) control loop

The digital data entering the FEE from DFACS can represent the amplitudes of the AC actuation waveforms or the DC voltages used for compensation of parasitic electrode voltages, TM charge measurement and discharge. The actuation amplitudes are converted by the digital controller into the required waveforms for each electrode and then added to the DC voltages. The resulting voltages are applied to the DAC in digital form. The actuation circuit concept can include only the forward (direct) path or also the feedback loop that includes a suitable attenuator and the ADC. In both cases, the higher resolution DFACS data shall be processed for the lower resolution DAC, which applies the resulting analog voltages to the DVA. The crucial circuit with respect to the low-frequency performance is the voltage reference used by the DAC and the (optional) ADC.

The DVA will have a variable gain because of very large dynamic range (up to 100 V_{RMS}) and limited DAC / ADC resolution. The DVA output is low-pass filtered with a minimum second order passive filter and applied through the sensing transformer primary winding to the electrode. The filtering is needed to remove possible spectral content around 100 kHz that could interfere with the sensing function. In addition to the filtering function, the actuation capacitor C_A is a low-impedance ground path for the sensing excitation currents at 100 kHz, flowing in opposite direction from the electrode to the sensing transformer.

The actuation block diagram also shows the resonance tuning capacitors C_R used in the sensing bridge. The electrodes and associated sensing and stray capacitances to the ground present a negligible current load to the actuation circuit. The resistors of the passive filters provide a short circuit protection in case the electrodes are shorted to the ground (e.g., via TM in case of direct contact).

3.3 Waveform Generator

As already stated in 3.1.5, the actuation waveforms must not change the zero DC potential on the TM and must be mutually orthogonal. Therefore, instead of applying DC voltages, one can apply either the bipolar pulsed DC voltages or the sinusoidal waveforms, both with zero average. For the former, a single frequency can be used for all pulsed signals and the orthogonality among different DOFs can be ensured through time separation of signals. For the sinusoidal waveforms, the signals can be simultaneously applied in time, but the orthogonality can be ensured using different frequencies. Both solutions are described in more detail in the next sections.

3.3.1 Pulsed Waveform Scheme

The simplest waveforms can be constructed with pulsed DC voltages as shown in Figure 3-3.

The x-φ DOF control with above waveforms is shown in Figure 3-1 for a better understanding. It is evident that the $\pm U_{1x}$ (front) and $\pm U_{2x}$ (rear) signals have zero average on all four electrodes in the first 6 waveform tick intervals, thus keeping zero DC voltage on the TM. Note that the U_{1x} signal resembles the cosine and U_{2x} the sine waveform. They are selected in this shape to be orthogonal, i.e., their product, when averaged on the 6 waveform tick interval, is zero. The same reasoning applies to other signals that are shifted in time. In total, 12 different control voltages are required: U_{1x}, U_{2x}, … , $U_{1\eta}$, $U_{2\eta}$ for translation and rotation, respectively.

While the application of DC pulses is beneficial because of simplicity, the biggest drawback of this scheme is the low duty cycle of the waveforms (1/9 in force and 1/3 in voltage) compared with the actuation with the DC voltages. This requires large voltage pulses to execute required forces and torques, which then requires larger power supply levels and increased power consumption.

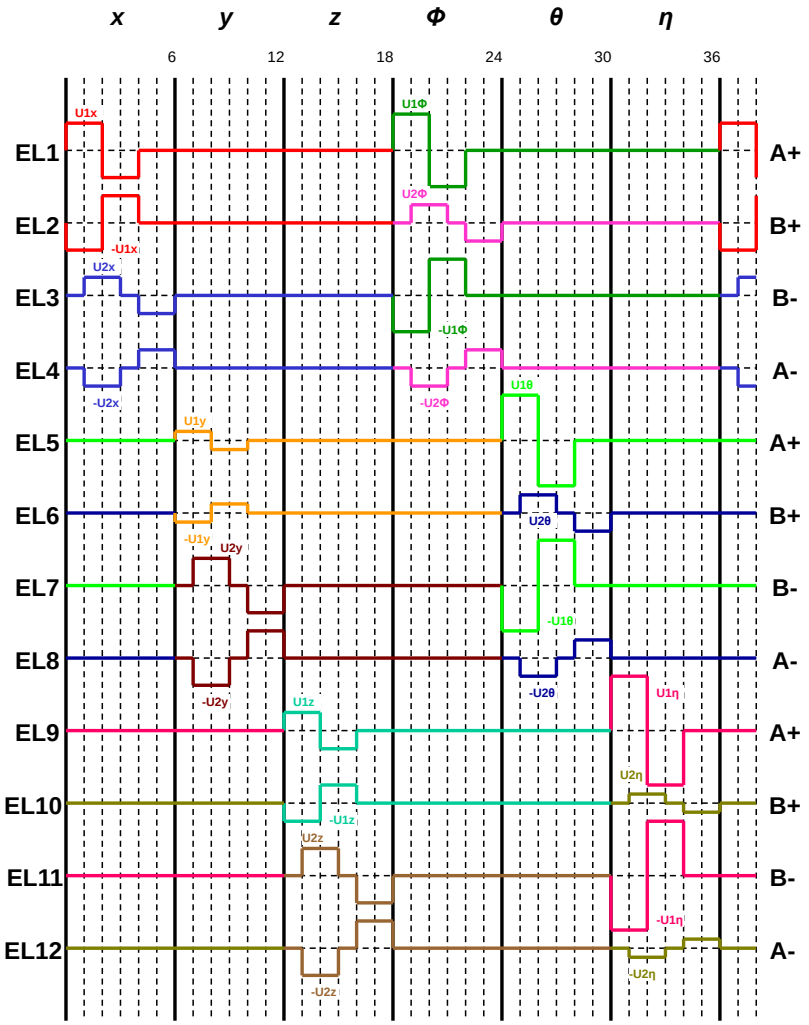

Figure 3-3 The pulsed actuation waveforms in time interleaved scheme for all 6 DOFs (x, y, z, φ, θ, η) applied on 12 electrodes surrounding the TM. A+ and B+ indicate the electrodes facing the front side of the TM, while A- and B- indicate the electrodes facing the rear side. Electrodes EL1-EL4 control the x-φ DOFs, EL5-EL8 the y-θ DOFs and EL9-EL12 the z-η DOFs. The numbers on top indicate time intervals in ms

3.3.2 Sinusoidal Waveform Scheme

The sinusoidal waveforms can be continuously applied, but with different frequencies for the 6 DOFs. Much like the pulsed waveforms, the front and rear waveforms are of different shape, e.g., sine and cosine signals. Since the actuation and sensing signals are simultaneously applied on electrodes, the actuation waveform frequencies must be selected such to prevent interference with the sensing function. This means that the actuation frequencies are not an integer factor of the sensing 100 kHz frequency. Their separation must also be higher than 20 Hz so as not to generate mixing low frequencies in the actuation baseband. To allow for some margin, a 30 Hz base frequency can be selected, from which the following higher harmonics derive for each DOF: 60 Hz, 90 Hz, 120 Hz, 180 Hz, 240 Hz and 270 Hz. The voltages on each electrode can thus be as follows:

$$\begin{aligned} EL_1 &= U_{1x}\sin(2\pi\cdot 60\cdot t) + U_{1\varphi}\sin(2\pi\cdot 270\cdot t) \\ EL_2 &= -U_{1x}\sin(2\pi\cdot 60\cdot t) + U_{2\varphi}\cos(2\pi\cdot 270\cdot t) \\ EL_3 &= U_{2x}\cos(2\pi\cdot 60\cdot t) - U_{1\varphi}\sin(2\pi\cdot 270\cdot t) \\ EL_4 &= -U_{2x}\cos(2\pi\cdot 60\cdot t) - U_{2\varphi}\cos(2\pi\cdot 270\cdot t) \end{aligned} \quad (3.11)$$

$$\begin{aligned} EL_5 &= U_{1y}\sin(2\pi\cdot 90\cdot t) + U_{1\theta}\sin(2\pi\cdot 240\cdot t) \\ EL_6 &= -U_{1y}\sin(2\pi\cdot 90\cdot t) + U_{2\theta}\cos(2\pi\cdot 240\cdot t) \\ EL_7 &= U_{2y}\cos(2\pi\cdot 90\cdot t) - U_{1\theta}\sin(2\pi\cdot 240\cdot t) \\ EL_8 &= -U_{2y}\cos(2\pi\cdot 90\cdot t) - U_{2\theta}\cos(2\pi\cdot 240\cdot t) \end{aligned} \quad (3.12)$$

$$\begin{aligned} EL_9 &= U_{1z}\sin(2\pi\cdot 120\cdot t) + U_{1\eta}\sin(2\pi\cdot 180\cdot t) \\ EL_{10} &= -U_{1z}\sin(2\pi\cdot 120\cdot t) + U_{2\eta}\cos(2\pi\cdot 180\cdot t) \\ EL_{11} &= U_{2z}\cos(2\pi\cdot 120\cdot t) - U_{1\eta}\sin(2\pi\cdot 180\cdot t) \\ EL_{12} &= -U_{2z}\cos(2\pi\cdot 120\cdot t) - U_{2\eta}\cos(2\pi\cdot 180\cdot t) \end{aligned} \quad (3.13)$$

Note that the frequency ratio on four electrodes is never an integer and that maximum frequency separation is taken for the most sensitive *x*-φ DOFs.

The duty cycle of the sinusoidal actuation compared with the actuation with the DC voltages is 1/2 in force and $1/\sqrt{2}$ in voltage, i.e., the voltage level that shall be taken for conversion into force is the RMS level – not the peak level. The ratio between duty cycles of two actuation schemes $(3/\sqrt{2} = 2{,}12)$ is the factor by which voltages can be smaller with sinusoidal actuation scheme, which finally sets the preference for the sinusoidal scheme. The drawback is more computation and memory required in digital electronics (look-up tables).

3.3.3 Actuation Voltages

The comparison between the two actuation schemes is given in Table 3-4 for the required actuation levels of the HR mode.

Table 3-4 Required TM translational and rotational accelerations for HR mode and their corresponding peak actuation voltages for the pulsed and sinusoidal actuation schemes

DOF	Required maximum acceleration a or α	Pulsed waveform peak voltage	Sinusoidal waveform peak voltage
x	$1{,}3\,\frac{\mathrm{nm}}{\mathrm{s}^2}$	8,9 V	4,2 V
y	$2{,}2\,\frac{\mathrm{nm}}{\mathrm{s}^2}$	11,6 V	5,5 V
z	$3{,}7\,\frac{\mathrm{nm}}{\mathrm{s}^2}$	19,3 V	9,1 V
φ	$16\,\frac{\mathrm{nrad}}{\mathrm{s}^2}$	5,6 V	2,7 V
θ	$27\,\frac{\mathrm{nrad}}{\mathrm{s}^2}$	6,2 V	2,9 V
η	$23\,\frac{\mathrm{nrad}}{\mathrm{s}^2}$	7,3 V	3,5 V

The conversion formulae between the acceleration and the actuation voltage can be easily calculated from (2.40), [51]. As an example, the *x*-φ acceleration to voltage conversion for sinusoidal waveforms are given by (3.14)

$$U_{x\_p} = \sqrt{2} \cdot U_{x\_rms} = \sqrt{2}\sqrt{m \cdot a_{x\_max} \frac{2d_x}{C_{2x}}} = 4{,}21\ V$$
$$U_{\varphi\_p} = \sqrt{2} \cdot U_{\varphi\_rms} = \sqrt{2}\sqrt{I \cdot \alpha_{\varphi\_max} \frac{2d_x}{C_{2x}R_\varphi}} = 2{,}68\ V \quad (3.14)$$

where mass and moment of inertia of the TM are m = 1,96 kg and $I = 691{,}2 \times 10^{-6}\ \mathrm{Nms^2}$, respectively, the *x*-axis electrode gap is d_x = 4 mm, the nominal capacitance of two electrodes on one side of the TM and the lever arm for torque calculation (half the distance between the centers of two electrodes on one TM face) are $C_{2x} = 2 \times 1{,}15$ pF and R_φ = 10,75 mm, respectively.

The requested actuation accelerations in the WR mode are much larger (Table 3-2) due to the large residual acceleration after the TM release by the caging mechanism. The switch to the HR mode is executed after the TM has stabilized enough so that the residual accelerations are below the actuation levels of the HR mode.

As already mentioned in 3.1.5, the constant stiffness actuation scheme is required only for the HR mode. This is because the stiffness augments with the square of the applied voltage, and keeping the constant stiffness scheme with large common voltages on electrodes for zero actuation could affect the control laws of the WR mode, i.e., the accelerometer operation mode. Therefore, a simpler actuation scheme is applied with voltages only on one side (corner) of the TM depending on the needed sign of translation (rotation).

In addition, the sinusoidal waveforms for force and torque are not simultaneously applied to limit maximum voltages on electrodes to 140 V peak. Instead, the force and torque are applied in the interleaved mode, every 100 ms (10 Hz). The result of this actuation scheme is the reduction of acceleration by half, i.e., the duty cycle of 0,5. Since the force and torques are split in time and the crosstalk is less important in this mode, the waveforms can be simplified having equal frequency, e.g., 120 Hz.

The WR mode acceleration to voltage conversion for e.g., *z*-η DOFs with sinusoidal actuation scheme are given by (3.15)

$$U_{z\_p} = \sqrt{2} \cdot U_{z\_rms} = \sqrt{2}\sqrt{m \frac{a_{z\_max}}{DUTY} \frac{2d_z}{C_{2z}}} = 140{,}7\ V$$
$$U_{\eta\_p} = \sqrt{2} \cdot U_{\eta\_rms} = \sqrt{2}\sqrt{I \frac{\alpha_{\eta\_max}}{DUTY} \frac{2d_z}{C_{2z}R_\eta}} = 139{,}8\ V \quad (3.15)$$

where DUTY = 0,5, d_z = 3,5 mm, $C_{2z} = 2 \times 0{,}61$ pF, R_η = 15,25 mm and maximum accelerations are specified in Table 3-2.

Similarly, the maximum WR actuation voltage levels for other DOFs can be calculated to be ≈ 141 V peak or 100 V RMS. This sets the constraints on the DVA and the sensing front-end design, e.g., in the selection of rating of the capacitors and the coaxial cables between the FEE and the electrodes. Note that to conform to the derating requirements for the space design, the voltage rating of the cables and the electronic parts must be at least twice higher than specified by the application.

3.4 Digital Controller

The actuation data calculated by DFACS can be the absolute peak amplitudes of the AC voltages, representing translational and rotational accelerations along each DOF and the DC electrode voltages. The AC voltages and different waveform schemes are described in previous sections. The DC voltages are used in three cases: for compensation of electrode stray voltages of ≈ 100 mV, for the TM charge measurement using slowly changing DC voltages, i.e., the dither of ≈ 1,5 V at 1 mHz and for the TM discharge with voltages up to 5 V. Therefore, the maximum DC level is set to ±5 V.

The block diagram of the digital and analog actuation circuits is shown in Figure 3-4. Since the DFACS is calculating the voltages with the 24-bit resolution and because the maximum voltage levels differ very much in HR and WR modes, the DFACS data are first adapted to the resolution of the hardware. The received AC voltages are then converted into the sine and cosine waveforms with correct frequencies and properly summed with the DC voltages for each electrode. The calculated total composite waveform command is then finally applied to the controller. As already stated in 3.2, the actuation control can be with or without the feedback. The design of the individual blocks is discussed in the next sections.

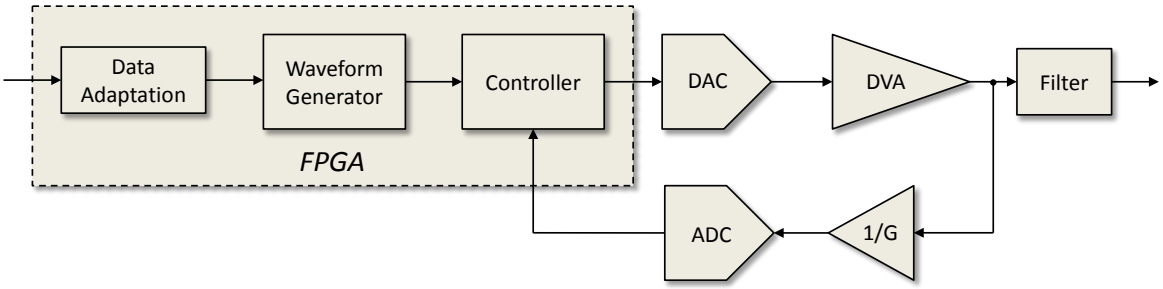

Figure 3-4 The block diagram of the actuation digital circuits and the analog circuits

The data adaptation is actually the truncation of the high-resolution DFACS data to a lower resolution, as shown in Figure 3-5 for both modes. Although the input is at a 24-bit resolution, only a 19-bit resolution in HR mode will suffice to achieve satisfying results of the DFACS control in the HR mode [52]. This means that there are no quantization limit-cycles in the low frequency control of the TM.

The space qualified ADC and DAC parts with more than 16 bits are still in the development or qualification process. Therefore, this truncation is mandatory and other solutions must be used to improve the resolution. At the time of writing, the octal 24-bit ADC ADS1278 from Texas Instruments was being tested on radiation by the manufacturer. If finally successful, it could be used in the feedback path and thus allow using the full DFACS resolution. Note that in this design the DAC does not need to be with more than 16 bits.

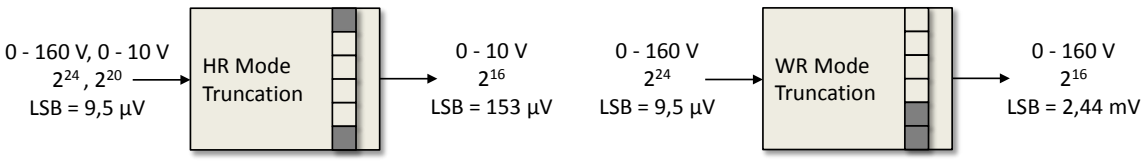

Figure 3-5 The truncation of the actuation data to match the resolution of the hardware in the HR and WR modes of operation. Each box represents one data nibble (half byte)

Since the maximum peak AC actuation voltages are approximately 140 V in the WR mode, the full scale range (FSR) of the amplitude command is chosen to be 160 V. It is provided to FEE in 24 bits, thus having the least significant bit (LSB) resolution of 9,5 µV. Note that in

the HR mode the FSR can be 10 V (maximum voltage is U_z = 9,1 V) and thus 16 times smaller. This means that in the HR mode the actuation voltages fit in 20 bits, as shown in Figure 3-5 with the gray color indicating the most (top) significant nibble (4 bits), which are zero.

In the HR mode the least significant nibble of the 20-bit command is removed in the baseline design of the controller to achieve the final 16-bit input command with a resolution of 153 µV. In the WR mode all 24 bits are used and the adaptation block removes the whole least significant byte (8 bits) of the command, again to achieve 16 bits with a resolution of 2,44 mV. Since the WR mode is not the scientific mode, the worsening of the resolution is not critical.

Two types of the digital controller will be described in the following text: the proportional, integral and derivative (PID) controller and the pulse width modulation (PWM) controller. Both controllers aim to improve the resolution beyond 16 bits of the hardware parts.

3.4.1 PID Controller

One controller channel, designated to one electrode, is shown in Figure 3-6.

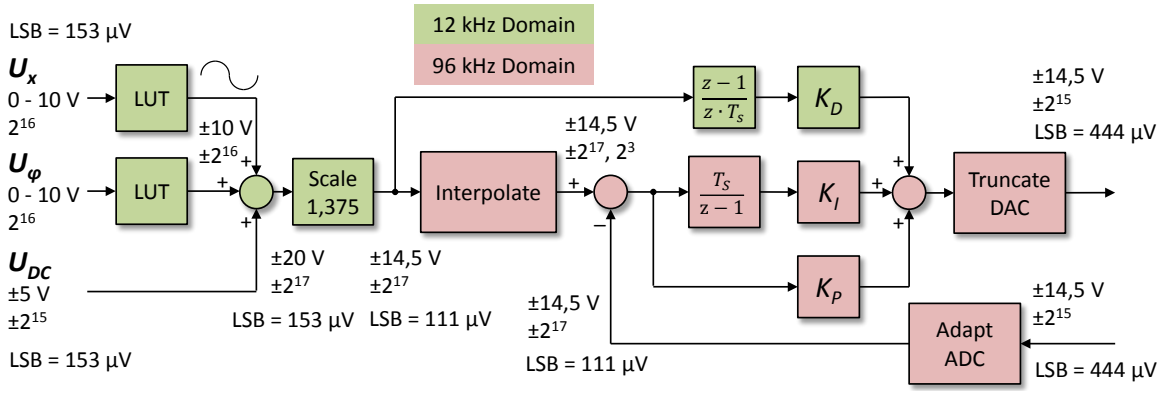

Figure 3-6 The block diagram of the PID controller with the sinusoidal waveform generator

The whole controller consists of the waveform generator based on a look-up table (LUT), the waveform combiner and the PID controller with forward and feedback blocks. It is obvious that it is sufficient to store only the levels of one quarter period of the unity sine waveform to generate both sine and cosine complete waveforms. In addition, since all waveform frequencies (60 Hz to 270 Hz) are the multiples of the 30 Hz base frequency, the samples of all waveforms at higher frequencies can be selected from the range of stored 30 Hz samples.

Note that one cannot directly compare the truncated input command of 16 bits with the 16-bit hardware. The AC amplitude input is unipolar, which requires one more bit for the bipolar waveform in the generator and in addition, the sum of AC and DC commands enlarges the FSR and thus the number of bits. Therefore, the 16-bit input requires minimum 18 bits for the controller (17 bits value plus sign), as shown in Figure 3-6.

Note that the AC and DC commands do not need to sum up with their full range. In particular, maximum 5 V DC level for the TM discharge will never be used simultaneously with the maximum AC actuation. At most, 1,5 V DC will be used for the simultaneous charge measurement. Therefore, by adding *z-η* actuation levels (Table 3-4) and the 1,5 V DC, the maximum needed level is 14,1 V, for which the ±14,5 V FSR and ±15 V power supply is suggested.

To accommodate the input LSB size (153 µV) on ±20 V FSR with the feedback ADC LSB (444 µV) on ±14,5 V FSR, the input command is scaled by a factor 1,375 to the LSB of 111

μV. The ratio of four between the size of the hardware LSB and the controller LSB also simplifies the controller feedback adaptation.

The selection of the waveform generator tick (sample) frequency follows two rules: its higher harmonic must not coincide with the sensing 100 kHz frequency, and its ratio with the base waveform frequency must be an integer. The former is to prevent the actuation to sensing crosstalk and the latter to ensure an integer number of samples in the 30 Hz cycle in which all waveforms have an integer number of periods. The 12 kHz frequency is suggested because it is the one that can be easily derived from the main 24 MHz FPGA clock. Note that the main waveform amplitude update cycle is 10 Hz, although the FEE could support 30 Hz update cycle.

The PID controller has the differential block configured as a feed-forward control with the coefficient K_D and acting on the input signal, contrary to the integrator and the proportional block, which act on the error signal. Therefore, the differentiator is operating at a 12 kHz input sampling frequency. The feed-forward signal is used to speed-up the output. For this purpose, the differentiator is combined with an analog integrator after the DAC so that their actions cancel each other out and the resulting input signal appears directly on the analog circuit output. The gain imperfectness in the feed-forward cancellation processes is compensated by the PI control.

The PID controller shall operate at a high sampling frequency not only for the purpose of stability, but also to reduce the noise by spreading the noise power to higher frequencies. In this respect, the control loop acts as a sigma-delta loop. To shift the input 12 kHz signal sampling to higher frequency, an interpolator that adds eight samples is inserted before the controller. The resulting controller frequency is 96 kHz, which is “very far” from the very narrow sensing band of 100 kHz ± 5 Hz and thus safe to prevent crosstalk. The interpolation acts as a division by eight and thus improves the resolution by three more bits, which are shown in Figure 3-6 by a 17-bit integer and 3-bit decimal value added by the interpolator.

It is important to note that the interpolator output waveform, in spite of having a very fine absolute amplitude resolution of 20 bit, is still only accurate to 16-bit in amplitude due to the input truncation. As an option, one could keep all 20 bits received from the DFACS and enlarge all FPGA registers by 4 bits, but because the controller output is truncated to a 15-bit value anyway, the improvement is not obvious. This option is discussed in 3.4.3.

The controller error is calculated by subtracting the feedback ADC value from the interpolated command. Since the ADC has only a 15-bit amplitude resolution and the input is at 17-bit, two zero bits shall be added to align the values. The ADC output is noisy, which acts as a dither and helps the controller to average between the low resolution ADC codes. The proportional and the integrated controller error are amplified by the corresponding coefficients K_P and K_I, and added to the feed-forward. To prevent the saturation of data (integration and addition), the number of bits used by the controller can further increase, but it will finally be truncated to ±15-bit at the DAC input because of its FSR.

Since the control loop operates at a high frequency, the output noise, as a result of large ADC quantization noise due to its low resolution, can be considerably reduced and thus can satisfy the DC noise requirement $10\,\mu V/\sqrt{\mathrm{Hz}}$ (3.10). The quantization noise is a random process with spectral density given by

$$S_U^{1/2}(f) = \frac{LSB}{\sqrt{12 f_N}} = \frac{444\mu V}{\sqrt{12 \cdot 48kHz}} \approx 0{,}6\,\frac{\mu V}{\sqrt{Hz}} \tag{3.16}$$

where LSB is one ADC voltage quant referred to the actuation output, f_N is the Nyquist frequency and the $2f_N$ is the loop sampling frequency.

The noise quantization discussed above must be distinguished from the actuation amplitude quantization. The latter is limited by the input signal resolution, which is in the baseline design 153 µV. Since the controller operates with a resolution of 111 µV, the actuation output is expected to interpolate the commanded values with a maximum differential non-linearity (DNL) error of two controller LSBs, i.e., 220 µV. The analog part of the control loop is discussed in 3.5.

3.4.2 PWM Controller

The controller using the pulsed width modulation (PWM) can increase the resolution of the controller by varying (modulating) the LSB between zero and one state at a high frequency and thus change the duty cycle or the average of the LSB in one input cycle. To add *N* sub-bits, the PWM must operate at a 2^N times higher frequency than the input sampling frequency. The PWM controller does not need the feedback to improve the noise because the PWM will improve the DAC resolution and thus the quantization noise. The block diagram of the PWM controller is shown in Figure 3-7.

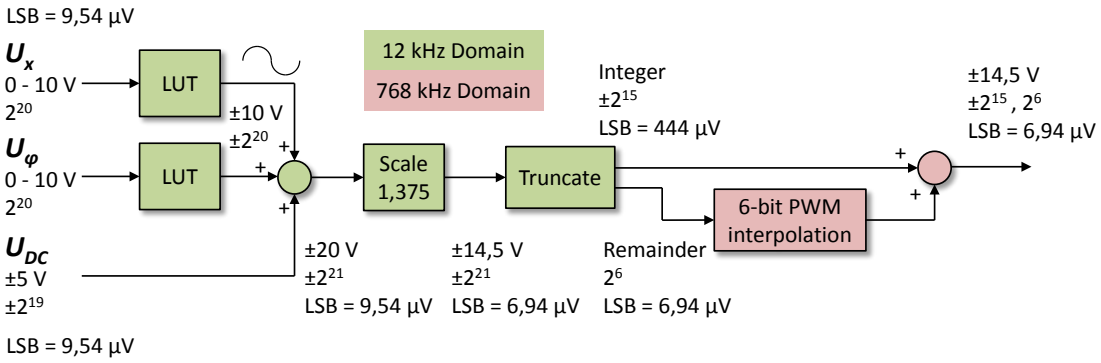

Figure 3-7 The block diagram of the PWM controller with the sinusoidal waveform generator

Compared with the PID controller, the input amplitudes are not truncated and the waveform generator operates on the full resolution of 22 bits (21-bit value and sign). Similarly, the composite waveform is scaled by factor 1,375 on ±14.5 V FSR, thus having a very fine resolution of 6,94 µV. Since the DAC is a 16-bit part, the input amplitude in 22 bits must be truncated. The six truncated bits must be recovered by the PWM, which requires the frequency ratio between the PWM and the waveform sampling frequency of $2^6 = 64$. If the same waveform frequency of 12 kHz (as in PID controller) is assumed, the PWM frequency is 768 kHz.

The PWM algorithm will in every 12 kHz time interval (83,3 µs) change the state of the LSB according to the remainder and thus achieve the LSB duty cycle from zero to 63/64. The algorithm will spread the PWM pulses to maximize the output variation, which is illustrated in Figure 3-8 on the simple PWM with only 8 states (3-bit interpolation).

A simple PWM algorithm, used to calculate when the pulse is generated in each cycle tick (1/768 kHz = 1,3 µs in our case) is shown in Figure 3-9. There are 64 ticks in every 12 kHz cycle and for each tick the algorithm is deciding if the output is to be one or zero.

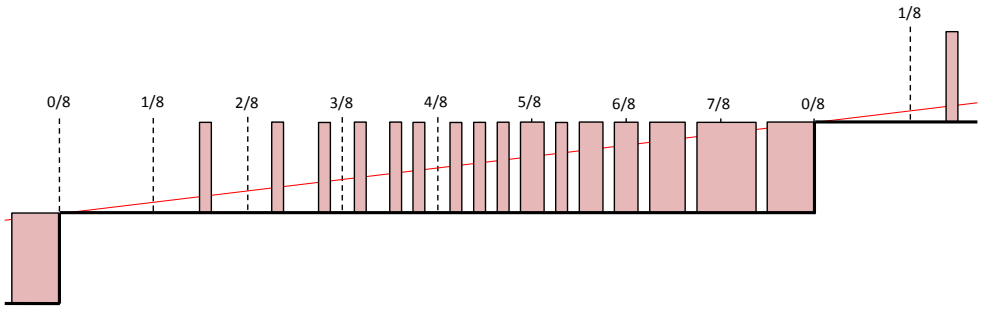

Figure 3-8 The example of a simple 3-bit PWM controller showing the output for a ramp input. The coarse output (in absence of PWM) is shown by the bold line and the sub-states are approximated with the pulses. The beginning of each cycle is indicated with the dashed lines and the corresponding duty cycle value

The algorithm starts by calculating the remainder expressed by 6 truncated bits, which are represented by the nominator of the duty cycle value shown in Figure 3-8. Then it places the pulses as symmetrically as possible against the center of the cycle so that the pattern is maintained over cycles with an equal input signal. This reduces the fluctuation of the average output. Every 64 cycles a new value arrives and the process repeats itself.

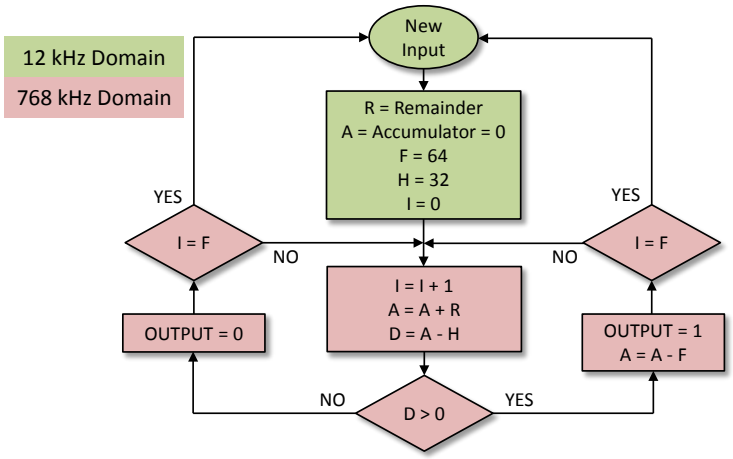

Figure 3-9 The PWM algorithm, which calculates the duty cycle and decides at which instant in time the pulse is generated (1) or not (0). It operates at 768 kHz, i.e., 64 times faster than the input data frequency

3.4.3 Controller Architecture Comparison

The PWM controller has a simpler architecture than the PID controller, i.e., it has no feedback. It is also more accurate as the input resolution of 9,5 µV is achieved by the time modulation of the coarse DAC level, whereas the PID controller has the input data truncated to the 153 µV resolution.

An improvement in the latter case is possible by keeping all 20 input bits like in the PWM case, expanding all registers by 4 bits and truncating the data after the interpolator (Figure 3-6). While this requires more FPGA recourses, it provides more accurate input to the PID controller block, which has potential for a more accurate output despite the low resolution of the ADC and DAC parts. Extending the full word length also to the PID block and then truncating just before the DAC would not improve the accuracy since the controller error is calculated from the very coarse ADC output. The simulation and analysis of the improved design [53] allows higher accuracy of the output, i.e., on average with 10 µV resolution. The

output setting accuracy is between 5 µV and 15 µV; that is a large improvement compared with the 100 µV to 200 µV accuracy of the baseline design with the truncated input.

The linearity of the actuation circuit depends on the DNL and the integral non-linearity (INL) of the DAC in PWM controller and the ADC in the PID controller. The suggested space-qualified parts are Linear Technology LTC1604A [47] for the ADC and Maxwell 7846A [54] for the DAC (commercial replacement is Analog Devices AD7846). Both parts have already been discussed in the sensing circuit (ADC) and the TM injection generator (DAC). Their parameters that are important for this analysis are given in Table 3-5.

Table 3-5 Linearity errors, speed and power of the LTC1604A ADC and the AD7846 DAC

Part number	DNL typical	DNL maximum	INL typical	INL maximum	Maximum Speed	Typical Power
LTC1604A	±0,3 LSB	±0,5 LSB	±0,5 LSB	±2 LSB	350 kHz	220 mW
7846A / AD7846	±0,35 LSB	±1 LSB	±1,5 LSB	±2 LSB	100 kHz	100 mW

As long as the DNL does not exceed 1 LSB, there will be no missing codes (ADC) or missing output voltages (DAC). The DAC performance is especially important in the PWM controller because there is no feedback. Furthermore, it is operating on the full scale in the PWM controller and only around zero in the PID controller.

While for the PID controller, the ADC and DAC speed is adequate for the suggested 96 kHz loop sampling frequency, the DAC maximum speed of 100 kHz appears too low for the PWM interpolation frequency of 768 kHz. In fact, the specified maximum speed is for the large signal, which is sufficient for the PWM signal sampling frequency of 12 kHz. The PWM interpolation frequency of 768 kHz relates to the variation of one LSB for which the suggested DAC has enough large bandwidth. The write cycle duration is about 300 ns, thus allowing the update faster than 2 MHz.

As there will be 12 actuation channels per TM, the power consumption is important. The suggested “low” power DAC (100 mW) seems to be an acceptable solution compared with e.g., a faster (30 MHz) space-qualified DAC with typical power of 465 mW. The noise performance of the ADC and the DAC are analyzed in 3.5.2. The dominating 1/f noise at low frequencies, in ADC / DAC internal analog circuits and external DVA circuits can be reduced by the chopping technique that is discussed in the next section.

3.4.4 Low-Frequency Noise Reduction

The analog circuits shown in Figure 3-2 and Figure 3-4 include the DVA, the low-pass filter and the ADC attenuator buffer in case of the PID architecture. To reduce the low-frequency noise, the analogue circuits following the PWM controller must include the chopper and the auto-zero operational amplifiers. As already mentioned in the PID controller description, the analogue circuit shall include the integrator, which works with the feed-forward differentiator of the digital controller and the feedback attenuator. Since the feedback ADC is the reference for the output, the low-frequency noise reduction will be implemented in the feedback circuit. Therefore, the buffer-attenuator operational amplifier must be an auto-zero type and the chopper will be placed before the ADC input to allow for noise reduction of the internal input analog circuits of the ADC. The chopping in analog circuits will be combined with the same function in the digital controller before the DAC or after the feedback ADC.

In the PWM architecture shown in Figure 3-10, one can digitally modulate the DAC input signal by switching its sign at some suitable frequency f_{CHOP}, e.g., at 12 kHz. The DAC output analog signal is first high-passed to remove the DAC offset fluctuation (1/f noise) and then inverted synchronously by an analog chopper. The chopper and the DVA must include the auto-zero buffers / amplifiers not to introduce the low-frequency noise.

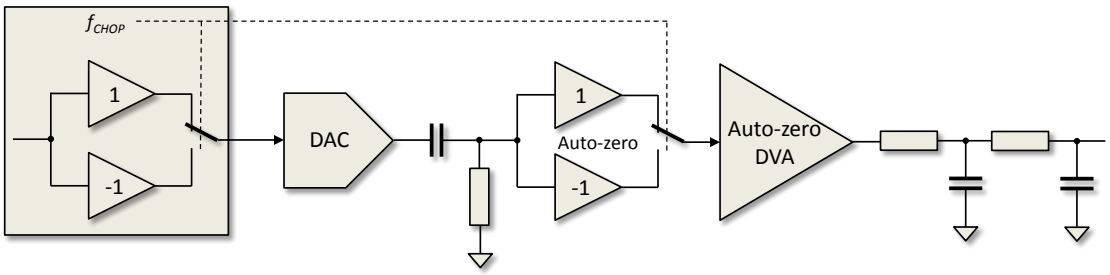

Figure 3-10 The low-frequency noise reduction scheme for the PWM based actuation circuit

In the PID architecture shown in Figure 3-11, the ADC analog input is modulated at a similar frequency by an analog chopper. The controller feedback signal is first digitally high-passed to remove the ADC offset fluctuation and then synchronously demodulated. Since the loop reference is the feedback ADC, only the chopper / attenuator buffers shall be of auto-zero type (and not the DVA).

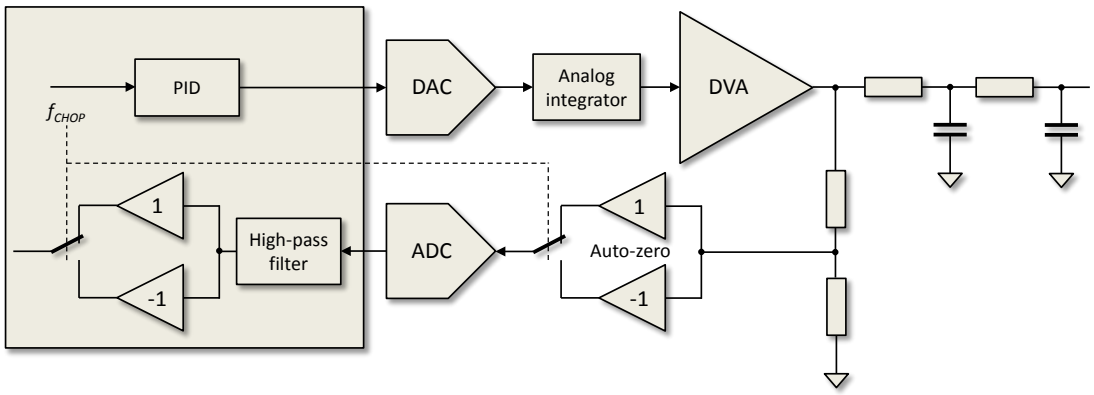

Figure 3-11 The low-frequency noise reduction scheme for the PID based actuation circuit

The actual design of the chopper for the PWM control circuit is shown in Figure 3-12.

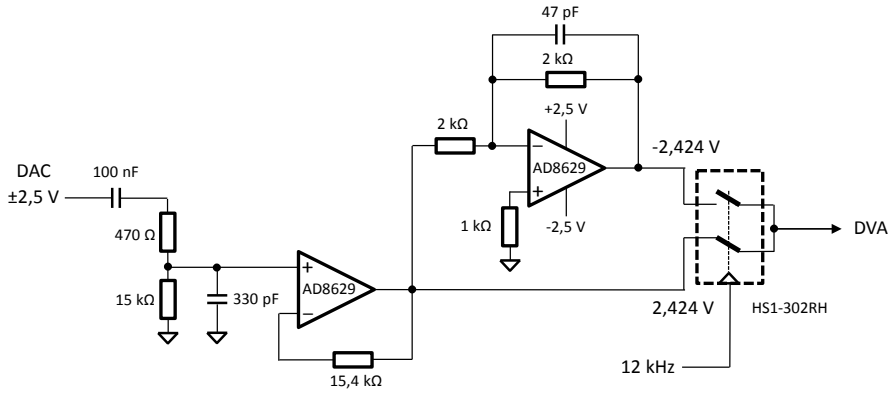

Figure 3-12 The chopper circuit that is used with the PWM controller and which is cancelling the low frequency offset fluctuation of the DAC

In the above circuit, the DAC output of ±2,5 V is reduced by factor 0,97 because the maximum power supply level of the auto-zero amplifier is ±2,5 V. Even though the AD8629

op-amp is the rail-to-rail amplifier, some headroom between the power rail and the FSR must be left to prevent saturation. Similar circuit for the low-frequency noise cancellation would be used in the PID feedback circuit.

3.5 Drive Voltage Amplifier

The drive voltage amplifier (DVA) is the DC amplifier amplifying and filtering the DAC output in the suitable bandwidth. The low-pass filter(s) corner frequency must be selected to pass the AC actuation signals without distortion and to sufficiently attenuate possible 100 kHz spectral content that could enter in the sensing circuit and generate the crosstalk.

The DVA must have its gain switchable and thus its output compatible with the FSR of the HR mode (±14,5 V) and the FSR of the WR mode (±145 V). The straight forward design would be to use the ±15 V power supply on the DVA operational amplifiers and the high-voltage power supplies of e.g., ±150 V on the transistor-based output driver. Note that the actuation voltages are connected to the TM electrodes providing the capacitive load of about 300 pF (C_R in Figure 3-2). The DVA output is also passively low-pass filtered using the filter resistors of several kΩ and the 10 nF capacitors (C_A in Figure 3-2). The filter resistors decouple DVA output from the capacitive load and serve as a short-circuit protection. Therefore, the DVA has to supply negligible current in normal operation and about 50 mA in the short-circuit condition at maximum output voltage of the WR mode.

Since the DC actuation is maximum ±5 V (for TM discharge), the high voltage output is only necessary for the AC actuation signals. This suffices to supply the DVA electronics with the standard ±15 V power supply and the use of the transformer to amplify the AC signals to ±140 V. An AC-DC splitter separating the composite waveforms into AC and DC parts and a passive R-C circuit to re-combine the amplified AC signal with the DC signal must also be included in this concept. This design has been suggested by the Swiss industry, responsible for the IS-FEE manufacturing and will not be discussed in this dissertation. Instead, the DVA design based on the high-voltage power supplies, suggested by the author of this dissertation, is described in the following section.

3.5.1 Transistor Based High-Voltage Driver

Many solutions exist in the literature dealing with boosting the limited op-amp output current or voltage driving capability. Several high-voltage designs, e.g., Figure 9 [55], [56] and Figure 6 [57], would be suitable for the DVA. The last one was the basis for the DVA circuit shown in Figure 3-13.

The DVA uses the dual auto-zero amplifiers AD8629 with the key parameters shown in Table 2-13. The first one is configured as a buffer separating the chopper analog switch (Figure 3-12) and the DVA gain selection switch. In the option with the PID controller, this amplifier must be configured as an inverting integrator. The second amplifier followed by the high-voltage transistor stage is the inverting amplifier with a switchable gain of G = 6 in the HR mode and G = 60 in the WR mode. The analog switch HS1-302HR, already discussed in 2.10.1, is used for the gain switching. It has typically 30 Ω series resistance and is open in the HR mode, thus preventing DVA gain variation due to its fluctuating series resistance.

The transistor driver's power supply is ±150 V. The DVA gain is adjusted to achieve an FSR output of ±14,54 V and ±145,4 V in the HR and WR modes, respectively. The first circuit stage made of complementary transistors in common base connection, Q1-Q2 is used to obtain the voltage gain. Transistors Q3 and Q4 provide additional gain to the Q7-Q8 complementary, emitter-follower output stage. Transistors Q5 and Q6 provide bias, while the diodes D3 and D4 minimize the crossover distortion of the last stage. Since the transistor

driver contains an inverting stage (Q3-Q4), the overall feedback is returned to the amplifier's non-inverting input. The 470 pF feedback capacitor provides the gain roll off and thus ensures an overall stability. The local AC feedback (15 kΩ and 470 pF) at the amplifier's inverting input provides the dynamic stability.

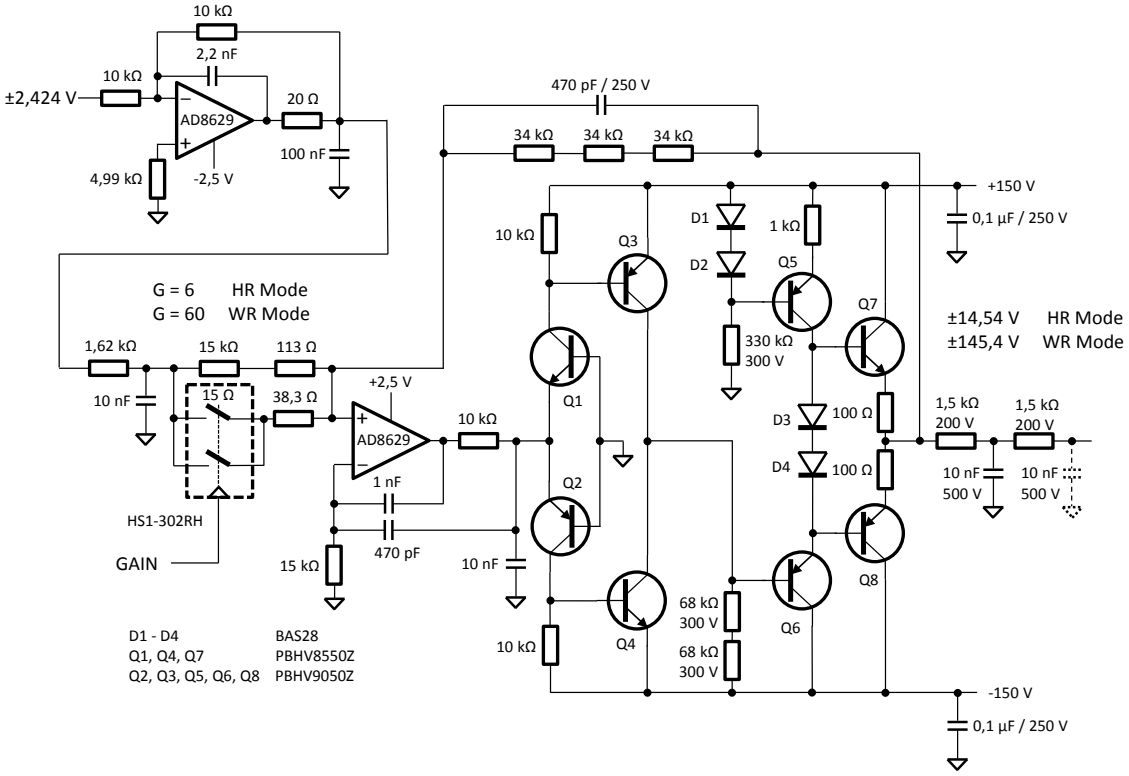

Figure 3-13 The DVA circuit including the dual auto-zero op-amp AD8629, the gain switching block, the transistor driving stage and the passive low-pass filter

The amplifier is loaded by the capacitor (10 nF) to provide additional filtering of the high-frequency auto-zero switching that is present at its output. To compensate the amplifier's phase due to capacitive loading, a standard compensation circuit is included in the inner amplifier's loop (1 nF and 10 kΩ). A similar circuit is implemented on the first amplifier.

The DVA circuit is followed by the 2nd order passive low-pass filter to reduce the spectral content at 100 kHz sensing frequency. The -3 dB corner frequency of the DVA driver, both stages of the passive filter and the overall DVA are 3,1 kHz, 4 kHz and 2,1 kHz, respectively.

The derating policy in space electronics requires that parts have a voltage rating twice as high as the maximum operating voltage. Since the transistors (U_{CE} or U_{CB}) are subject to almost 300 V peak operating voltage at the FSR of the WR mode, the transistors with 500 V rating are suggested. These are currently the highest voltage transistors available in the medium surface-mount package (SOT223). The transistor have a current rating of 0,25 A (PNP) and 0,45 A (NPN), but the passive filtering stage limits the short-circuit current to 50 mA. In the normal operation, the bias current (in absence of signal) of the output transistors is 0,75 mA. At the maximum waveform frequency of 270 Hz and the maximum signal level, the transistors have, in addition, a dynamic load of ±5 mA in the WR mode and ±0,25 mA in the HR mode. This dynamic load is due to the charge and discharge currents of the passive low-pass filter.

3.5.2 Noise Performance

The most important noise requirements are the actuation amplitude stability of the AC signal at the waveform frequency (60 Hz to 270 Hz) and the actuation DC noise in the measurement bandwidth (MBW < 1 Hz). The former is limited to $2\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ (3.6), i.e., $20\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ for the 10 V peak amplitude, and the latter to $10\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ (3.10).

The actuation instability is directly related to the instability of the voltage reference in the DAC circuit or in the feedback ADC circuit in case of the PID controller. The best space-qualified voltage reference, the LT1021 (Figure 2-16), has a low-frequency noise less than $2\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ only above 1 mHz. This would satisfy the LTP requirements, but not the LISA mission operating at 0,1 mHz. The LT1021 noise at this frequency is $4\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$, i.e., twice the limit. The stacking of four references would reduce the overall reference noise by half, assuming their noise is uncorrelated. The voltage reference MAX6126 from Maxim is not the space-qualified part but would fit the LISA requirements with its $1{,}5\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ noise at 0,1 mHz [58].

The MBW noise limit of $10\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ should be easily achieved if the low-frequency noise cancelation by the suggested chopping technique (3.4.4) is successfully implemented. The theoretical low-frequency noise of the auto-zero DVA design from Figure 3-13 is only $0{,}36\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$, according to the simulation result shown in Figure 3-14. The noise at 100 kHz is negligible.

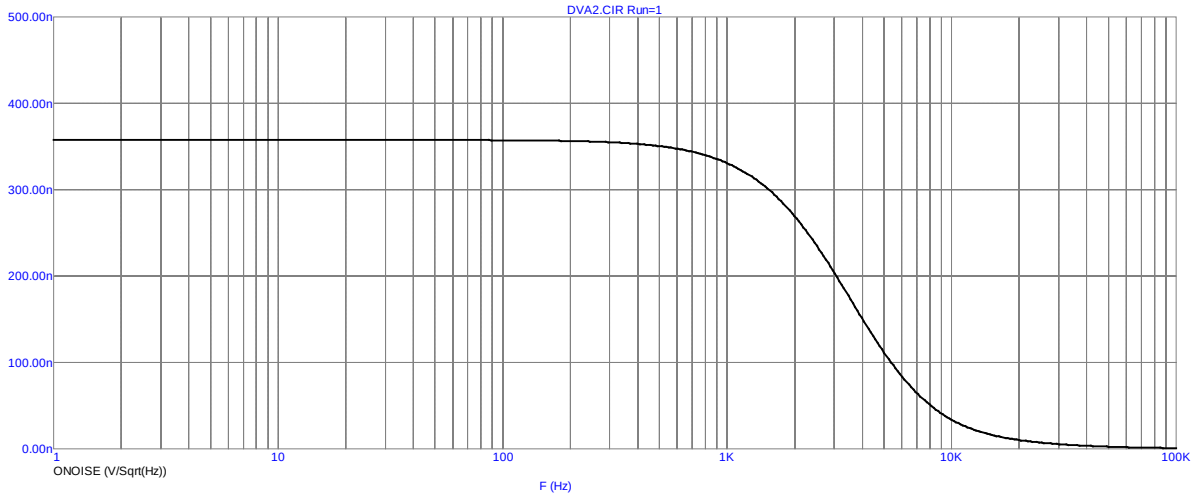

Figure 3-14 The DVA wideband noise with $0{,}36\,\mu V/\sqrt{Hz}$ *at 1 Hz and* $0{,}9\,nV/\sqrt{Hz}$ *at 100 kHz*

Chapter 4
BREADBOARD ELECTRONICS

During the IS-FEE development, many different prototype circuits, called breadboards, were realized to verify concepts and the detailed design. The results of the testing on these breadboards established the initial electronics design and were the basis for the transfer of knowhow to the Swiss industry. Later on, the industry investigated some new ideas and even though the main principle circuits remained the same, the flight electronics delivered by the industry did not strictly follow the designs described in this dissertation.

Not all circuits were realized during the breadboarding activity, e.g., some digital functions and ADC / DAC circuits were not implemented, because most of the challenges lay in analog electronics. The crucial circuits, described in the breadboard architecture, were built in several phases of the project, starting in 2004 with small breadboards of the essential IS-FEE circuits, continuing throughout 2005 with the building of the multi-axis breadboard electronics for the torsion pendulum in Trento, Italy, and finally in 2010 with the upgraded breadboard for the similar torsion pendulum in Florence, Italy. The major design goal in the initial phase was performance rather than the reduction of mass and power or the radiation issues. Therefore, the breadboards were made with commercial parts, some even not having the space-qualified counterparts at that time. The parts with space heritage that are usually based on old technologies, and thus worse performance, were analyzed for suitability in the breadboard. The implementation of strictly space-qualified parts would also largely affect the cost and the development time.

Only the final breadboard electronics built for the Universities of Trento and Florence will be described in the following sections with corresponding performance results.

4.1 Breadboard Architecture

The block diagram of the breadboard (BB) electronics is shown in Figure 4-1.

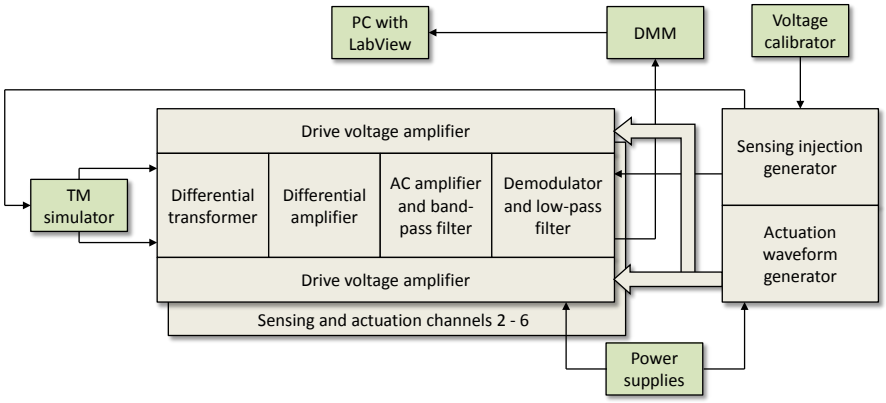

Figure 4-1 The breadboard electronics block diagram consisting of 6 sensing and actuation channels to control 12 electrodes and the main control board generating injection and actuation signals. The instrumentation consists of the Test Mass simulator, the DC voltage input generator (the calibrator), the power supplies and the digital voltmeter (DMM) with control, acquisition and analysis LabView software inside the personal computer (PC)

Although the diagram is self-explanatory, it is important to note that the voltages representing the actuation amplitudes and the TM injection bias amplitude are not delivered to the BB by a digital interface. Instead, the analog DC voltages are directly applied to the BB from a very stable voltage source (the voltage calibrator), thus eliminating the DAC circuits. Similarly,

the sensing outputs are not acquired by the onboard ADC circuits and delivered to PC via digital interface. Instead, the DMM or an acquisition ADC card acquires the analog outputs from the BB and sends digital measurement data to the PC. The implications of this simplification will be discussed in the measurement section.

The TM simulator is necessary to generate very stable differential capacitances of few femto Farads, which is not an easy task. Its design is described in 4.3.2.1. Two breadboard electronics built for the Universities of Trento and Florence follow the above architectural design and are shown in Figure 4-2. The core of the electronics is the sensing and actuation board shown in Figure 4-3. Sensing and actuation boards are stacked on top of each other while the main control board is at the very bottom. The main control board (Figure 4-28) is described in 4.4.2.

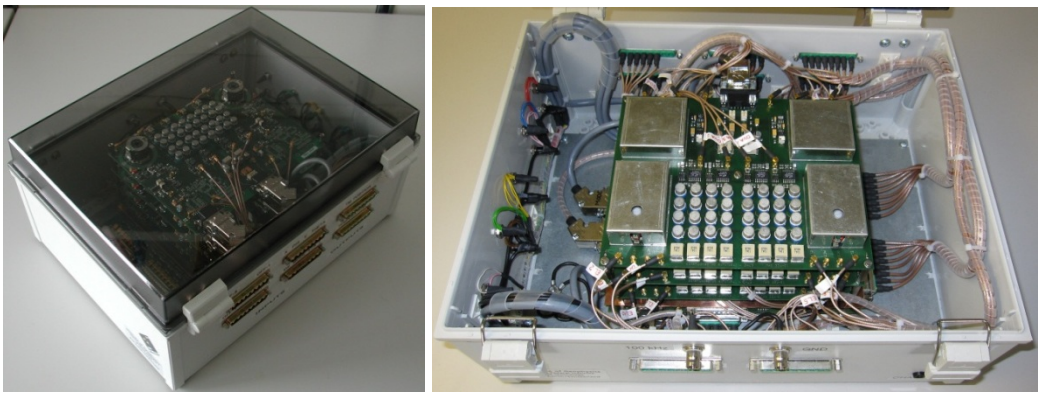

Figure 4-2 The IS-FEE breadboard electronics for the control of the torsion pendulum: the first model (left) was built in 2005 and the second (right) in 2010

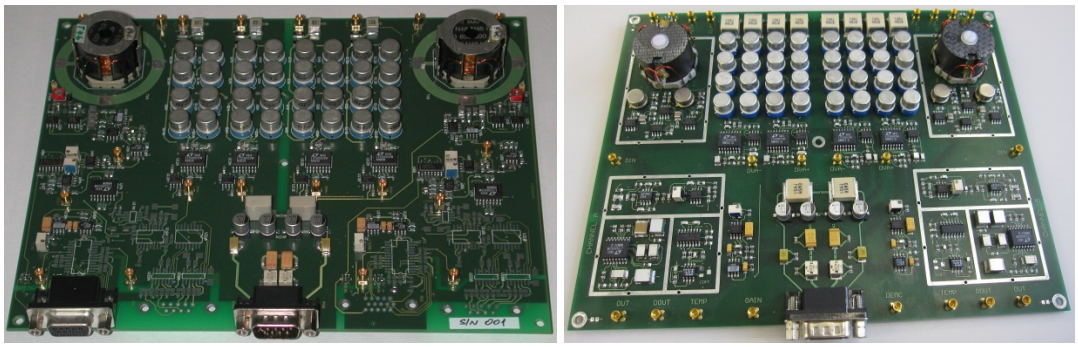

Figure 4-3 The first (left) and the second (right) sensing and actuation electronics assigned to four electrodes consisting of two sensing channels and four actuation channels. The parts not mounted in the left picture are the optional ADC and DAC circuits

The transformers with the front-end amplifiers are clearly visible in the upper part of Figure 4-3 (right), surrounded by the metal frame. The electronics below includes the band-pass filters, the demodulators and the output low-pass filters. Each DVA circuit in the middle consists of eight transistors and corresponding input amplifiers. The board power supply filtering section is above the power connector. The author of this dissertation designed all the circuits of both breadboards. The FPGA code development used in the second control board for the sinusoidal waveform generation was done by another engineer. The layout of the boards, the manufacturing of transformers, the assembly of the boards, the whole box assembly and the LabView programming for testing was done by a technician under close guidance of the author. The following sections describe in more detail the design and the measurement results.

4.2 Sensing Transformer Design and Measurements

The first attempt to design the sensing transformer was similar to the initial design of the UTN, i.e., a traditional transformer with manually or machine-wound windings on the plastic coil former. After successful development and achievement of very good results, the knowhow was transferred in 2005 to the space industrial partner who was able to achieve the same performance. To ensure higher resistance to the mechanical and thermal stress and to reduce the cost of manufacturing, the Swiss partner responsible for flight hardware development suggested a transformer with planar windings made inside the multi-layer printed circuit board (PCB). Following this idea, another version of the planar transformer was developed by the author in 2010 with slightly different coil artwork and made of Teflon-based PCB.

4.2.1 Traditional transformer

The transformer core selection and the coil design are discussed in 2.7.2 and 2.7.3, respectively. The expected performance and general winding guidelines are given in 2.7.4. During the transformer design activity, more than 30 different versions were built until satisfactory results were achieved in all design aspects. The experimenting included the following options:

- Ferrite core material N48 in P26x16 size, ungapped (A_L = 4900 nH) and gapped with A_L of 400 nH, 630 nH and 1000 nH
- Coil formers with one, two and three sections
- Copper wire with diameter of 0,1 mm, 0,15 mm and 0,2 mm
- Litz (stranded) wire with Polyurethane insulation 10/41 (10x0,07 mm) and 20/44 (20x0,05 mm)

The Litz wire, which helps reduce the skin effect, was quickly rejected because of its larger overall diameter, which required tight placement of wires in the coil former and thus much larger distributed capacitance (200 pF instead of requested 20 pF). In addition, this type of wire cannot be precisely positioned in the coil former, i.e., it is soft and causes crossovers between neighboring turns. With 100 turns per winding of Litz wire 20/44, the Q was maximum 240-270 around 20-30 kHz and only 50-60 at 100 kHz for two different gapped cores. The use of 10/41 Litz wire improved the results, but the distributed capacitance could not be reduced below 50 pF. Even though the Q between 220 and 250 was achieved at 100 kHz, the maximum Q of 380-450 was still peaking at lower frequencies of 40-50 kHz.

The single transformer copper wire insulated by lacquer (called also the magnet wire) allows better positioning in the coil former, but the distributed capacitance lower than 40 pF could not be reached with either a 0,2 mm of 0,15 mm wire diameter. Therefore, the experimenting continued with the spaced turns on each layer. This was done by simultaneously winding two wires of 0,15 mm diameter next to each other and then by removing one winding. This made it possible to achieve a distributed capacitance of 18 pF for the first time and a very good Q of 365 and 470 at 100 kHz for cores with A_L of 400 nH and 630 nH, respectively. The maximum Q of 400 and 520 was now peaking at 140 kHz and 80 kHz, respectively. By fine-tuning the number of turns, one can achieve a maximum Q of around 100 kHz. The reduction of the wire diameter to 0,1 mm increased the DC resistance of the winding considerably, e.g., from previously 3,8 Ω to 12 Ω. Therefore, further experiments continued with the 0,15 mm wire.

Double and triple section (chamber) coil formers allow a low stray capacitance between primary windings because each winding is wound in its own section. The lowest capacitance

was 8 pF and was achieved with a double section coil former. On the other hand, a single section coil former has the largest winding volume because the walls of additional sections reduce usable volume. The coil formers with more sections also reduce the ability to wind two primary windings symmetrically.

The experimenting with different coil formers aimed to reduce the inductance asymmetry between two primary coils, which was at first around 8000 ppm instead of the required 50 ppm. The straightforward method of winding to achieve very good symmetry would be the bifilar winding (simultaneous winding of two coils). With this method of winding one can only use the single section coil former. While this really improves the initial symmetry (30-120 ppm), the stray capacitance between two primary windings becomes very large because two coils are wound side by side [59]. This capacitance can be as large as 730 pF with tight winding and 190 pF with spacing.

Large primary to primary winding capacitance in the sensing circuit is added to the distributed capacitance of each primary coil, which thus requires a much smaller external resonance tuning capacitance or shorter coaxial cables for the 100 kHz resonance. In addition, Q is drastically reduced to 80. Note that until the transformer is placed in the circuit, the distributed capacitance of the primary winding is low (30 pF) and Q is high (300). The bifilar transformer symmetry can easier be fine-tuned by axial positioning of the coil former in the core down to 5 ppm. Since bifilar winding generates a large distributed capacitance in the sensing circuit, it has been abandoned.

Experimenting with different cores showed that only cores with A_L of 400 nH and 630 nH were feasible. With a 1000 nH core and an ungapped (4900 nH) core, one could only achieve Q to peak at 65 kHz and 60 kHz, respectively.

The symmetry tuning between two primary windings was experimented on all types of coil former. The winding using the single section coil former and thus the second primary winding on top of the first one, i.e., not in the same layer, generates a huge asymmetry. A small displacement of the two primary windings relative to the core gap (by thin spacers under the coil former) changes the relative magnetic couplings and thus the output in the secondary winding. This method has been used to fine-tune the symmetry.

The double section coil former dedicated to each primary winding reduces the initial asymmetry, but its tuning by axial positioning of the coil former in the core makes very large positive or negative asymmetry, i.e., it is very coarse. To overcome this problem, both primary windings were wound in both sections of the coil former by first winding 50% and then crossing and winding the remaining 50% in the other section. This allowed very fine tuning, but also some reduction of Q to 220 due to a larger stray capacitance between two windings (22 pF). By reducing the percentage of the winding that is crossed on the double section coil former, a compromise was found with Q = 240 and less fine tuning capability.

Finally, the triple section coil former has been chosen; see the winding sketch shown in Figure 2-25. The transformer parts and assembled transformer are shown in Figure 4-4.

The winding parameters are provided in Table 4-1 and a summary of the measurements on transformer in Table 4-2. The transformer Q transfer functions are shown in Figure 4-5.

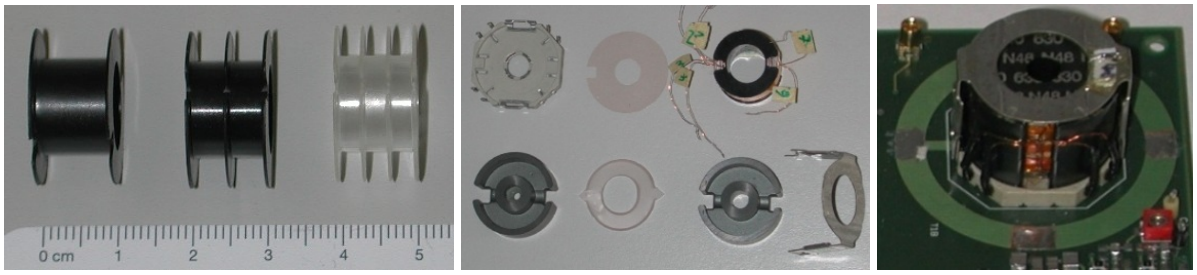

Figure 4-4 The coil formers used during transformer design (left), the disassembled (middle) and the assembled (right) transformer

Table 4-1 Transformer parameters

Parameter	Value
Core size	P26x16
Core material	Ferrite N48
Inductance factor A_L of gapped core	630 nH
Coil former type	3 sections
Wire (copper) diameter	0,15 mm
Number of layers in primary winding	4 + 2 (crossed)
Number of turns per layer (primary)	14 and 12 (crossed)
Number of layers in secondary winding	5
Number of turns per layer (secondary)	16
Number of turns per each winding	80
Spacing between turns in each layer	none
Spacing between nominal and crossed winding	1,76 mm
Spacing below the secondary winding	1,6 mm

Table 4-2 Measurements of relevant transformer parameters

Parameter	Value	Guidelines
DC resistance (primary)	4,18 Ω	3,9 Ω
DC resistance (secondary)	4,46 Ω	
Inductance (primary)	4,28 mH	4,03 mH
Inductance (secondary)	4,24 mH	
Self-resonant frequency (primary)	710 kHz	> 400 kHz
Self-resonant frequency (secondary)	711 kHz	
Distributed capacitance (primary)	11,8 pF	< 40 pF
Distributed capacitance (secondary)	11,7 pF	
Primary to primary stray capacitance	13 pF	< 20 pF
Primary to secondary stray capacitance	9,6 pF	
Q of the primary winding at 100 kHz	375 - 425	> 200
Q of the secondary winding at 100 kHz	360	
Transformer symmetry	< 15 ppm	< 50 ppm

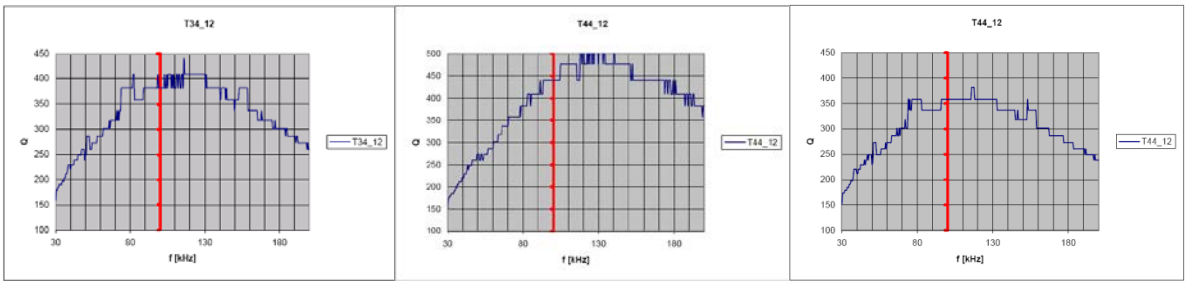

Figure 4-5 The Q transfer functions of the primary windings for the final ETHZ transformer (left) and the transformer made by an industrial partner following the same design, before (middle) and after (right) impregnation

The measurements show that Q is peaking around 120-130 kHz with a value of up to 500 and that the impregnation is reducing it to 350. The curve is flatter after impregnation and is well positioned around 100 kHz. It was found that the impregnation affected the symmetry tuning, making it 10-20 times worse. Probable reasons are:

- The coil former might have changed shape due to the dry out procedure under high temperature and caused a slight displacement within the core (w.r.t. the air gap)
- The lacquer that flew inside the windings changed the winding capacitance
- The lacquer inside the core changed the inter-winding capacitance

Since the transformer symmetry requirement of 50 ppm is set 20 times lower than the equivalent 1 µm sensing offset requirement and because it can be, in addition, compensated by the asymmetric selection of the actuation filter capacitors ($C_{a1,2}$ in Figure A-1), the observed detuning of the transformer asymmetry was deemed not problematic.

When the transformer is inserted in the sensing circuit, the quality factor of the whole sensing bridge can decrease from the standalone transformer measurement. A different distribution of the stray capacitances when all three windings are connected in the bridge circuit and the quality factor (losses) of the resonance tuning capacitors, placed in parallel to the primary windings, can affect the overall quality factor. Note that only the quality factor of the primary windings affects the bridge performance and not of the secondary winding.

4.2.2 Planar transformer

As already mentioned in the introduction in 4.2, the planar transformer was developed by another Swiss institute, the University of Applied Sciences of Western Switzerland (HES-SO). Each winding of the planar transformer also has 80 turns. Several turns are made per plane in an elliptical shape, which are then paralleled by other planes of the multi-layer PCB and mutually connected by the PCB through-hole vias to make one winding. The windings made this way do not require a coil former, as the PCB size is cut exactly to the required shape to fit inside the Ferrite cores. The secondary winding is part of the main sensing and actuation PCB and two primary windings, separately manufactured, are glued with spacers on each side of the secondary winding. The cores are then adjusted vertically relative to the winding stack and finally glued to a supporting flange mounted on the main PCB.

A larger dielectric constant (permittivity) of the PCB material (4,4 for the Arlon 35N) in the planar transformer, compared with the air (~1) and Teflon insulation (2,1) in the traditional transformer causes a larger stray capacitance between its layers and thus a lower Q, i.e. > 20 pF and 200, respectively. The design of HES-SO was the basis for the modified planar transformer in the second IS-FEE BB, which is shown in Figure 4-6.

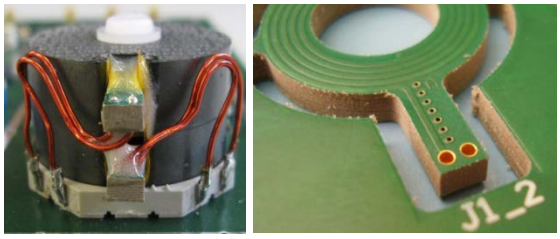

Figure 4-6 The assembled ETHZ planar transformer (left) and its winding design (right)

Several design modifications have been made in an attempt to reduce stray capacitance:

- The transformer windings have been built from the high-frequency PCB material based on the ceramic-filled Teflon (PTFE) laminates TSM-29 with the dielectric constant of 2,94 (eight double-side laminates stacked to achieve 16-layer PCB)
- The through-hole vias, previously occupying the circular coil area, have been replaced by the buried vias in each of eight laminates to connect their upper and bottom sides. This created free space in the circular area of the coil
- Seven through-hole vias were still needed to connect laminates together, but this has been done in an extension that does not limit the area for the winding tracks (Figure 4-6)
- With more space for winding, the width of the track was enlarged to reduce DC resistance
- The top and bottom winding artwork on each layer is displaced so that the overlap area is minimized and the capacitance thus reduced
- The PCB winding is slightly thicker (≈ 3.1 mm) to enlarge the distance between the layers and thus reduce the distributed capacitance
- Each PCB winding is separated by a Teflon spacer that does not cover the whole winding area to maximize the area where the air is separating the windings. This also reduces stray capacitance between the windings
- All three windings are glued together with corresponding Teflon spacers and then assembled with the transformer cores. After assembly in the circuit, the sensing offset is only roughly tuned by the movement of the PCB winding stack inside the ferrite core and then glued to the core. Then the actuation capacitors in the sensing circuit are fine tuned to achieve the required sensing offset

The comparison of the measurements on both types of transformers is provided in Table 4-3.

Table 4-3 Measurements on the planar transformer and the traditional transformer. Better performance is highlighted in green

Parameter	Planar	Traditional
DC resistance (primary)	3,13 Ω	4,18 Ω
DC resistance (secondary)	3,18 Ω	4,46 Ω
Inductance (primary)	4,24 mH	4,28 mH
Inductance (secondary)	4,03 mH	4,24 mH
Self-resonant frequency (primary)	562 kHz	710 kHz
Self-resonant frequency (secondary)	562 kHz	711 kHz
Distributed capacitance (primary)	18,9 pF	11,8 pF
Distributed capacitance (secondary)	19,9 pF	11,7 pF
Primary to primary stray capacitance	11,6 pF	13 pF
Primary to secondary stray capacitance	11,9 pF	9,6 pF
Q of the primary winding at 100 kHz	251	375 - 425
Q of the secondary winding at 100 kHz	227	360

The maximum quality factor of the planar transformer is 260 and has its peak at 70 kHz. The DC resistance decreased as expected, the stray capacitances between the windings were about the same, but distributed capacitance was higher and consequently the self-resonant frequency lower. This has a visible impact on the quality factor *Q*, which dropped considerably, although it was above the minimum required (200). Distributed capacitance is slightly better than the one measured on the similar transformer made by HES-SO (20 pF), which means that the Teflon PCB material cannot reduce the distributed capacitance.

Despite the considerable effort in the redesign, the performance of the planar transformer in the sensing application cannot be matched with that of the traditionally wound transformer, but both satisfy the IS-FEE requirements.

4.3 Sensing Circuit Design and Improvements

The sensing circuit design and noise analysis were discussed in great detail in sections 2.8 to 2.11. The goal of building the breadboard was to confirm the theoretical noise analysis with measurements. In 2004 and 2005, when the prototyping took place, there were slightly different IS-FEE requirements than the current ones discussed in section 2.3, but they did not change the principal performance goals. At that time, the HR full-scale sensing range was ±100 µm instead of ±200 µm, and the actuation scheme was based on the pulsed waveforms with maximum ±100 V instead of the sine waveforms with a maximum peak voltage of 140 V. In addition, several electronic space-qualified parts were not available at that time, e.g., auto-zero amplifiers. The breadboard was also built with some "modern" commercial parts promising best performance instead of traditional parts with space flying heritage. The power supply levels were selected according to the chosen parts and are not equal to the levels needed for the parts in the design described in sections 2.8 to 2.11.

To comply with the ±100 µm HR range (≈ 60 fF), the preamplifier circuit, consisting of the differential TIA and the AC amplifier, was first designed as shown in Figure 4-7.

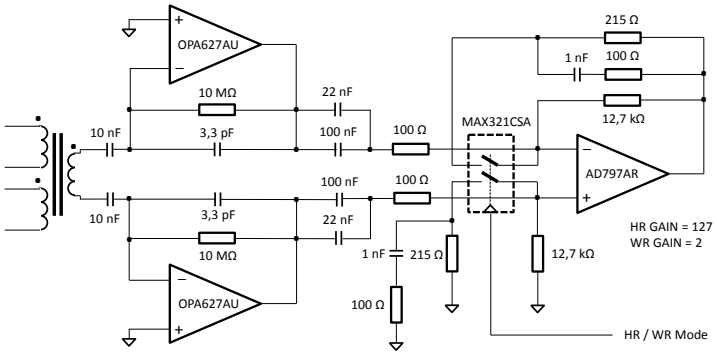

Figure 4-7 The front-end circuit of the first IS-FEE breadboard

The gain of the trans-impedance stage is defined by the feedback capacitance of 3,3 pF and can be written from (2.92) as

$$G_{TIA} = \frac{U_O}{\Delta C} = K\frac{C_a}{C_a + C_p}\cdot\frac{2U_M}{C_{FB}} \cong 2\frac{U_M}{C_{FB}} \tag{4.1}$$

where U_O is the differential TIA output, ΔC is the measured capacitance, K is the transformer coupling between primary and secondary windings, U_M is the TM bias voltage, and C_a, C_p and C_{FB} are the actuation, resonance tuning and feedback capacitances, respectively. The factor 2 is because of a differential TIA circuit. The factor $K\,C_a/(C_a + C_p)$ is approximately 0,92 and can be ignored here.

The block diagram of the whole sensing chain in the first IS-FEE breadboard is shown in Figure 4-8. The band-pass filter and the synchronous phase detector (demodulator) design follows, in principle, the designs shown in Figure 2-33 and Figure 2-35, respectively. The band-pass filter initially had a simpler design with a wide pass band from 20 kHz to 600 kHz and a gain of 1,33. The demodulator has been built with the LTC1051 auto-zero amplifiers instead of the recently available space qualified AD8629 zero-drift amplifiers. The different power supply levels of these amplifiers and the full HR output sensing range of ±5 V, selected for the digital acquisition cards (not part of IS-FEE), were the drivers for the gain selection of the circuit. Note that the factor $2/\pi$ in the detector circuit is due to the averaging of the fully rectified AC signal. Therefore, the total signal gain after the TIA is G_S = 211 and the noise gain is G_N = 298.

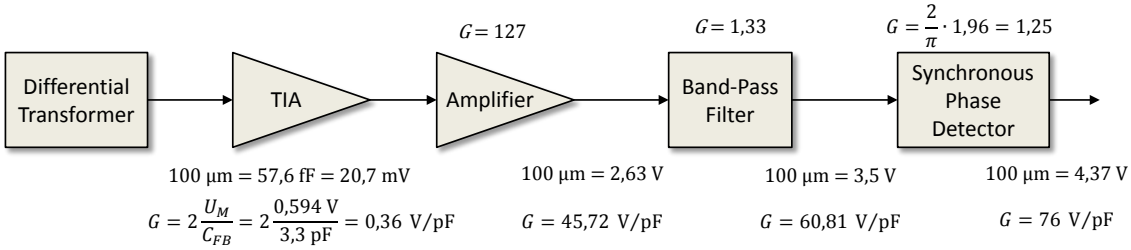

Figure 4-8 The sensing chain of the first IS-FEE breadboard designed for the ±100 µm range

The noise gain includes additional factor $\sqrt{2}$ by which the noise density is enlarged due to the demodulation process, as explained in 2.10. There it was assumed that the demodulation process using either the mixer or the analog switch provides the same result. For the former, the mixer with twice larger reference amplitude is used to compensate the demodulator gain reduction by a factor of two after demodulation. For the latter, the analog switch generating fully rectified output, and the low-pass filter averaging this output with the gain loss of $2/\pi$, is compensated by an additional gain of $\pi/2$ (1,57) at the output amplifier. In both cases the DC output represents the peak of the input AC signal. The additional gain after the demodulator circuit (in our case 1,25) does not change the SNR and thus the effect of the noise enlargement, before/after demodulation, by factor $\sqrt{2}$.

4.3.1 Sensing Noise at Zero Test Mass Position

The best sensing noise performance can be achieved when the TM is centered between the sensing electrodes, i.e., when sensing capacitance ΔC is zero. This is because the amplitude stability of the TM sensing injection bias (100 kHz) is rejected due to multiplication by the zero ΔC (Figure 2-12). In the testing campaign this is easily simulated by disconnecting the injection bias from the TM or setting it to zero. One caution shall be raised though: having the TM in the center and thus equal common mode sensing currents through both sensing transformer windings is not the same as having zero common mode currents when injection bias is zero. These two measurement methods are valid only if the instability of the bridge parameters is negligible and the grounding in the sensing circuit and connecting cables is proper, i.e., no ground loops. Since it is very difficult to manufacture the zero TM position simulator with the capacitance difference of < 100 aF in its two arms, the measurement method with zero injection bias was commonly used. More on the TM simulator design can be found in 4.3.2.1.

The testing campaign was documented by several technical notes (TN) written by the author of this dissertation, which will be referenced as needed in the following text. Additional design and sensing noise analyses, also written in several TNs and related to the flight electronics design, are not the subject of this dissertation.

The first noise measurements shown in Figure 4-9 pointed to excess noise against the theoretical calculations even though the results were satisfactory, i.e., the noise was at the limit (with the actuation circuit disconnected) or marginally above (with connected actuation circuit) [60]. With the IS-FEE sensing output gain of 76 V/pF and the sensing noise limit of $1\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$, the sensing noise limit expressed in voltage is $76\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$. The measurements during the debugging campaign showed that the actuation circuit contributed with about $5\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ of the total noise and that the true sensing noise contribution was around $83\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$.

The noise will be dominated by the sensing bridge thermal noise, as shown in Figure 2-31. Assuming the worst case bridge quality factor Q = 200, the theoretical noise shall be 73% of the limit and even lower with the achieved transformer Q of > 300 (Table 4-2).

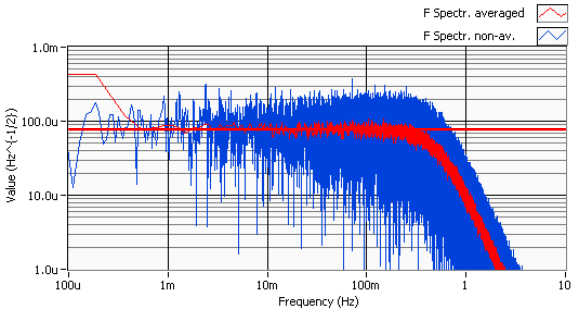

Figure 4-9 The sensing noise of the first IS-FEE breadboard of $83\,\mu V/\sqrt{Hz}$ is slightly above the sensing noise limit of $76\,\mu V/\sqrt{Hz}$ indicated by the red line

The conducted investigation [60], [61] ended with the following conclusions:

- The sensing noise is dominated by the TIA circuit and not by the transformer bridge (left plot in Figure 4-10)
- The bridge quality factor is larger than initially estimated, i.e., Q > 250 (middle plot in Figure 4-10)
- The circuits following the TIA introduce negligible noise (right plot in Figure 4-10)
- The origin of excess noise: either the TIA op-amp has a larger noise current [60] at 100 kHz and thus is not equal to the specified one at 100 Hz, or the input capacitance [61] of the TIA op-amp increases the noise gain

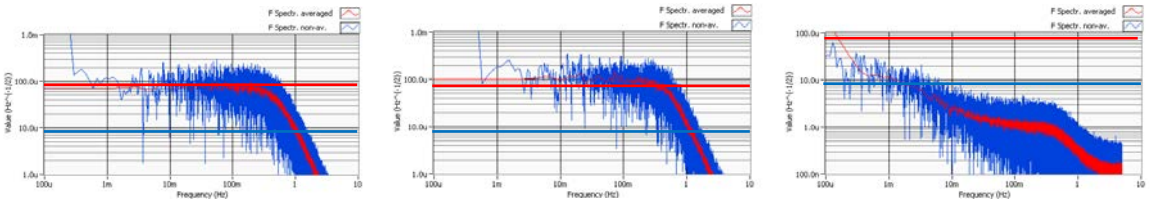

Figure 4-10 The sensing noise of $70\,\mu V/\sqrt{Hz}$ with disconnected transformer bridge, i.e., open TIA input (left), the $100\,\mu V/\sqrt{Hz}$ sensing noise using the 665 kΩ resistor equivalent to the transformer bridge of Q = 250 (middle) and the sensing noise of the AC amplifier, filter and the demodulator circuits after the TIA (right). In all cases the sensing limit of $76\,\mu V/\sqrt{Hz}$ is indicated by the red line and the theoretical TIA limit of $8{,}5\,\mu V/\sqrt{Hz}$ by the blue line

The elaboration of these findings is given in the following paragraphs. Note that the noise gain factor $\sqrt{2}$ due to the demodulation process was not considered in the initial analysis in 2006, even though this contribution was detected and discussed with respect to the signal gain.

4.3.1.1 The op-amp current noise

The measurement in the configuration with the disconnected transformer bridge (left plot in Figure 4-10) shows the noise level slightly below the limit, i.e., at about $70\ \mu V/\sqrt{Hz}$. With the parameters of the TIA op-amp OPA627 [62], listed also in Table 2-15, the noise of the differential TIA in open condition should not exceed $8{,}5\ \mu V/\sqrt{Hz}$. The TIA current noise of only $1{,}6\ fA/\sqrt{Hz}$ can generate negligible noise on the feedback impedance (Figure 2-31) consisting of 10 MΩ resistance and the 3,3 pF capacitance (Figure 4-7), which is 482 kΩ at 100 kHz. The current noise from the data sheet [62] is given only for 100 Hz, but the plot of the total harmonic distortion and noise (THD+N), showing the linear increase of noise beyond 200 Hz towards higher frequencies, indicates that the current noise is much larger at 100 kHz. In fact, an increase of 110 times is expected from this plot, i.e., $275\ fA/\sqrt{Hz}$ if using the maximum noise level at 100 Hz of $2{,}5\ fA/\sqrt{Hz}$. Also indicative is the SPICE simulation model of the OPA627, which has a current noise of $53\ fA/\sqrt{Hz}$.

Further investigation [61] by varying the TIA feedback impedance allowed estimation of true current noise in the op-amp, which is provided in Table 4-4. The experiment was conducted with only one TIA op-amp in the circuit and in its open input configuration, for which the dominating noise sources were the current noise through the feedback impedance and the thermal noise of the real part of the feedback impedance. During the experiment the TIA feedback capacitance was kept at nominal value. The table shows the best fit with the measurements when the OPA627 current noise is modeled with $335\ fA/\sqrt{Hz}$. The TIA voltage noise is modeled with $5\ nV/\sqrt{Hz}$ and the post-TIA noise gain is $211 \cdot \sqrt{2} = 298$.

Table 4-4 Calculated and measured sensing noise with single TIA in open input configuration and OPA627 op-amp modeled with $335\ fA/\sqrt{Hz}$ *current noise and* $5\ nV/\sqrt{Hz}$ *voltage noise*

R_{FB}	$\lvert Z_{FB}\rvert$	$\Re[Z_{FB}]$	Current noise	Thermal noise	TIA noise	Modeled output noise	Measured output noise
10 MΩ	481,7 kΩ	23,2 kΩ	161,4 $\frac{nV}{\sqrt{Hz}}$	19,6 $\frac{nV}{\sqrt{Hz}}$	162,6 $\frac{nV}{\sqrt{Hz}}$	48,5 $\frac{\mu V}{\sqrt{Hz}}$	50 $\frac{\mu V}{\sqrt{Hz}}$
1 MΩ	434,4 kΩ	188,7 kΩ	145,5 $\frac{nV}{\sqrt{Hz}}$	55,9 $\frac{nV}{\sqrt{Hz}}$	156,0 $\frac{nV}{\sqrt{Hz}}$	46,5 $\frac{\mu V}{\sqrt{Hz}}$	45 $\frac{\mu V}{\sqrt{Hz}}$
100 kΩ	97,9 kΩ	95,9 kΩ	32,8 $\frac{nV}{\sqrt{Hz}}$	39,9 $\frac{nV}{\sqrt{Hz}}$	51,9 $\frac{nV}{\sqrt{Hz}}$	15,5 $\frac{\mu V}{\sqrt{Hz}}$	15 $\frac{\mu V}{\sqrt{Hz}}$
10 kΩ	10 kΩ	10 kΩ	3,4 $\frac{nV}{\sqrt{Hz}}$	12,9 $\frac{nV}{\sqrt{Hz}}$	14,2 $\frac{nV}{\sqrt{Hz}}$	4,35 $\frac{\mu V}{\sqrt{Hz}}$	4,3 $\frac{\mu V}{\sqrt{Hz}}$
1 kΩ	1 kΩ	1 kΩ	0,3 $\frac{nV}{\sqrt{Hz}}$	4,1 $\frac{nV}{\sqrt{Hz}}$	6,5 $\frac{nV}{\sqrt{Hz}}$	2,2 $\frac{\mu V}{\sqrt{Hz}}$	1,9 $\frac{\mu V}{\sqrt{Hz}}$
0	0	0	0	0	5 $\frac{nV}{\sqrt{Hz}}$	1,8 $\frac{\mu V}{\sqrt{Hz}}$	1,7 $\frac{\mu V}{\sqrt{Hz}}$

Good agreement between the model and the measurements (last two columns) confirms that the excess noise is caused by the op-amp current noise. The modeled value is also not far from the one estimated through the THD+N plot.

It has already been mentioned that the noise of the open TIA circuit was about $70\ \mu V/\sqrt{Hz}$. Dividing this noise by the noise gain of 298, the differential TIA noise at its output is $235\ nV/\sqrt{Hz}$, which must be generated by the op-amp noise current of $345\ fA/\sqrt{Hz}$ on $\sqrt{2} \cdot 482$ kΩ feedback impedance of two op-amps (being the reason for factor $\sqrt{2}$). This again confirms the $335\ fA/\sqrt{Hz}$ modeled value for the current noise.

4.3.1.2 The bridge quality factor

The initial pessimistic estimate for the sensing transformer bridge quality factor was $Q = 250$. This quality factor with the transformer inductance of L = 4,24 mH generates an equivalent

bridge output impedance of 666 kΩ at 100 kHz, as calculated by (2.23). The measurement shown by the middle plot in Figure 4-10, using the 665 kΩ resistance in place of the equivalent transformer bridge impedance, indicates the noise of 100 $\mu V/\sqrt{Hz}$, which is larger than expected. Namely, the TIA noise contribution referred to the sensing output, and being dominated by the 335 $fA/\sqrt{Hz}$ current noise, shall be about 69 $\mu V/\sqrt{Hz}$ while the bridge thermal noise simulated by R_{BR} = 665 kΩ resistance, also referred to the output, shall be by (4.2) equivalent to 45,3 $\mu V/\sqrt{Hz}$. From these two values the total noise should have been 82,5 $\mu V/\sqrt{Hz}$ and not 100 $\mu V/\sqrt{Hz}$.

$$e_{BR\_TH} = \sqrt{4k_BT \cdot R_{BR}} \cdot 2\frac{|Z_{FB}|}{R_{BR}} \cdot 298 = 45{,}3\frac{\mu V}{\sqrt{Hz}} \tag{4.2}$$

In (4.2) the factor $2|Z_{FB}|/R_{BR}$ is the inverting differential TIA signal gain (2.91) and factor 298 is the noise gain after the TIA. The difference in the expected and measured noise comes from the wrong estimation of *Q*.

The total sensing noise was reduced by some initial modification described in 4.3.1.3 from 80 – 85 $\mu V/\sqrt{Hz}$ to 75 – 80 $\mu V/\sqrt{Hz}$, i.e., by 6% [60]. The measurement noise on the open TIA input also reduced from 75 $\mu V/\sqrt{Hz}$ to 70 $\mu V/\sqrt{Hz}$ due to this modification. It is difficult to determine the level of the noise from the ASD and to draw conclusions about the bridge quality factor, but the best estimate for the total sensing noise at 0,1 Hz could be 78 – 79 $\mu V/\sqrt{Hz}$ (Figure 4-11).

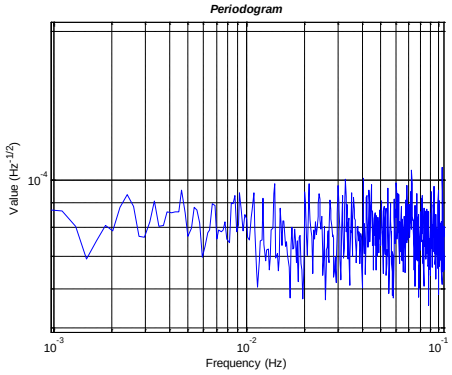

Figure 4-11 The sensing noise by band-pass filter modification: 78 – 79 $\mu V/\sqrt{Hz}$ *at 0,1 Hz*

Using the 78 – 79 $\mu V/\sqrt{Hz}$ values and the 70 $\mu V/\sqrt{Hz}$ value generated only by TIA, the bridge thermal noise contribution can be calculated to be between 34,4 $\mu V/\sqrt{Hz}$ and 36,6 $\mu V/\sqrt{Hz}$. The bridge resistance is then from (4.2) either 1155 kΩ or 1020 kΩ, which is then from (2.23) equivalent to the bridge quality factors of 434 and 383, respectively. For further analysis, the average is taken equal to Q = 409, R_{BR} = 1088 kΩ and the bridge thermal noise equal to e_{BR_TH} = 35,5 $\mu V/\sqrt{Hz}$. The estimated quality factor is similar to the measurements of the transformer alone, as shown in Figure 4-5.

Even though the most important sensing design parameter, the sensing bridge quality factor, can be compliant with the requirements, the major incompliancy of the TIA noise had to be solved. The activities and measurements on the improved sensing circuit, in particular on the TIA front-end, are therefore explained in the next section.

4.3.1.3 Initial sensing circuit improvements

Besides the TIA excess noise, the performance of the band-pass filter and the demodulator was investigated during the test campaign [60]. To reduce a possible leakage of the out-of-band noise into the demodulator circuit, the band-pass filter was modified by reducing its

pass band and thus attenuating the frequencies around a sensing 100 kHz carrier frequency more. The pass band was reduced from 20 kHz – 600 kHz to 89 kHz – 132 kHz using a design similar to the one suggested in Figure 2-34. The simulation [60] showed that the large noise below the 100 kHz was greatly reduced by the new filter (Figure 4-12). The ratio between the maximum out-of-band noise and the noise at 100 kHz at the demodulator input was thus reduced by 3,4 times compared with the previous filter. The result of this modification was a reduction of the total noise by 5-6%, i.e., to $79\ \mu V/\sqrt{Hz}$. The TIA contribution was also reduced by 6-7%, i.e., to $70\ \mu V/\sqrt{Hz}$. Since the improvement is not large, the conclusion is that the demodulator is working fine even under presence of large out-of-band noise.

The stray peak at 100 kHz was also found in the sensing spectrum (Figure 4-12), causing an offset of 29 mV, which was considerable compared with the offset limit of 1 µm = 44 mV. It was found that the analog switch in the demodulator circuit, operating at 100 kHz, was radiating noise, which was picked-up by the nearby TIA circuit. A large grounded copper shield (Figure 4-13) helped completely remove the stray peak and reduced the offset to only 68 µV. The shielding was later improved in the second BB by guard rings around each circuit (Figure 4-3) and metal covers (Figure 4-2). The improved shielding reduced the sensing noise by another 5%, i.e., to $75\ \mu V/\sqrt{Hz}$. The noise due to the TIA contribution, following this modification, was not measured.

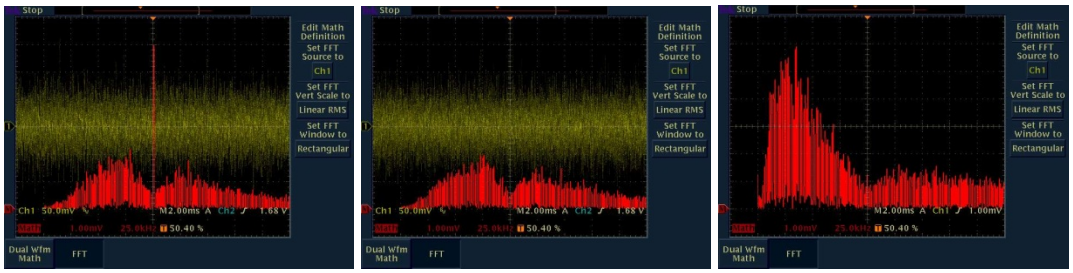

Figure 4-12 The band-pass filter output spectrum for unshielded demodulator analog switch causing stray peak at 100 kHz (left), shielded analog switch (middle) and the original wide band-pass filter with large out-off-band noise below 100 kHz (right)

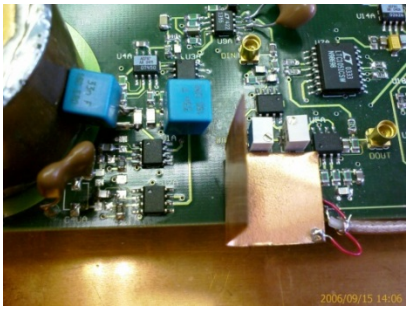

Figure 4-13 The shielded analog switch of the demodulator (under the copper shield) was introducing noise into the two trans-impedance op-amps located under two large blue capacitors. In the second BB these two circuits are largely separated and carefully shielded

4.3.1.4 Discrete TIA front-end

Once the reason for the TIA excess noise was found in the large current noise of the OPA627, a new front-end design with the discrete junction field effect transistors (JFET) was analyzed and proposed [61]. It must be noted that the OPA627 input capacitance of 15 pF was also investigated in 2006 and by coincidence it appeared that could also explain the excess noise.

In fact, the analysis with the input capacitance would be valid for the sensing bridge output impedance that is constant and resistive, which is not the case with the transformer bridge (Figure 2-7). Further on, the theoretical analysis of the TIA noise gain in APPENDIX C shows that the TIA input capacitance is added to the distributed capacitance of the secondary winding, can then be transferred to an equivalent additional capacitance on the primary winding and added to the resonance tuning capacitors attached to the transformer primary winding. Even though the op-amp input capacitance changes the frequency at which the bridge resonates and where the TIA noise gain has its minimum, it does not influence the noise since the bridge is always tuned by its capacitors for a minimum noise at 100 kHz. These two characteristic frequencies are slightly shifted, but the tuning for the minimum noise can be achieved in an acceptable manner [63].

The modified schematic of the TIA front-end is shown in Figure 4-14 and its realization in Figure 4-15. The JFETs are added in the circuit for two reasons. First, to decouple the OPA627 inputs from the large 10 MΩ feedback resistance and thus force the op-amp large noise current to flow through the parallel combination of the 10 kΩ external JFET source resistance and the 100 Ω internal JFET drain-source resistance r_{DS}, where it can generate negligible voltage noise on the TIA output. Second, to replace the OPA627 large input capacitance from the transformer secondary winding (via 3.3 nF decoupling capacitance) with smaller JFET input capacitance.

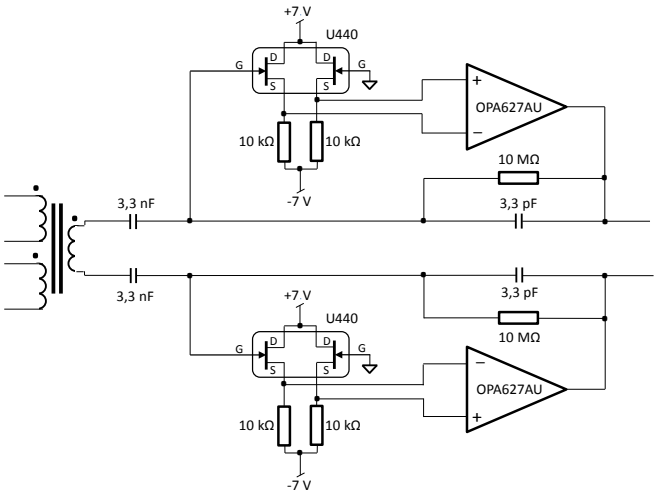

Figure 4-14 The modified TIA circuit schematic in the first IS-FEE breadboard

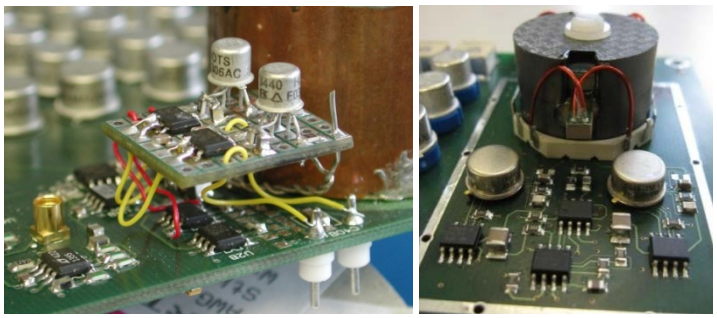

Figure 4-15 The retrofit of the sensing front-end circuit in the first IS-FEE breadboard with the U440 JFETs (left) and the appropriate redesign implemented in the second IS-FEE breadboard with the U421 JFETs (right)

The author of this dissertation suggested a similar modification of the front stage for the IS-FEE design made by HES-SO (previously called HEVs), which was simulated and discussed

in more detail during the initial flight electronics development [64], [65]. The JFET configuration (Figure 4-14), where JFETs operate as buffers, compared with the inverting amplifier configuration, where op-amps are connected to the JFET drain [65], provides less sensitivity to the circuit parameter fluctuation.

The JFETs types that would fit in the design are listed in Table 4-5. It must be stressed that the discrete stage was only needed because of late discovery of the excess current on OPA627. The space qualified FET op-amp RH/LT1056 (Table 2-27) would not require the discrete input stage. It was not tested because the OPA627 was the preferred part with wider bandwidth (BW). The influence of the op-amp BW to the TIA transfer function is shown in APPENDIX B.

Table 4-5 Parameters of different dual JFETs suitable for the TIA front-end design

Part number	Cut-off voltage $\lvert U_{GS\ (off)}\rvert$	Leakage current $\lvert I_{GSS}\rvert$	Drain current I_{DSS}	Input capacitance C_{ISS} (C_{GS})	Reverse capacitance C_{RSS} (C_{GD})	Voltage noise e_N
U421	0,4-2 V	0,6 pA	0,06-1 mA	3 pF	0,6 pF	10 $\frac{nV}{\sqrt{Hz}}$
U440	1-6 V	1 pA	6-30 mA	3 pF	1,7 pF	4 $\frac{nV}{\sqrt{Hz}}$
2N4393DCSM	0,5-3 V	5 pA	5-30 mA	13 pF	7,5 pF	1,3 $\frac{nV}{\sqrt{Hz}}$
2N5196	0,7-4 V	10 pA	0,7-7 mA	3 pF	1,5 pF	9 $\frac{nV}{\sqrt{Hz}}$
U401	0,5-2,5 V	2 pA	0,5-10 mA	8 pF	1,8 pF	2,5 $\frac{nV}{\sqrt{Hz}}$

The JFET 2N4393DCSM, with the largest input capacitance, is the space-qualified part that is selected for the flight hardware. For the remaining two on the list, the radiation test reports show up to 10 krad and 5 krad total dose compliance. The first two JFETs on the list are used on the second and the first BB, respectively. Note that the U421 is the low drain current JFET compared with the other types.

The noise calculation of the front-end circuit with JFETs is analyzed in [63] for the slightly different design. The noise model of the modified TIA input stage is analytically derived in APPENDIX D.

The theoretical calculations and the measurements [61] are in very good agreement. The measurement results of the complete circuit and the circuit with the open TIA are shown in Figure 4-16 and Figure 4-17, respectively.

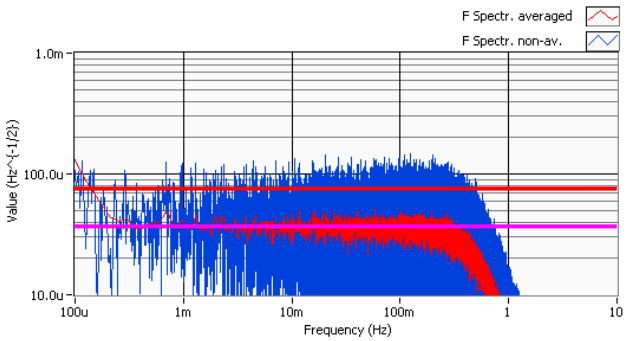

Figure 4-16 The noise of the complete sensing circuit after modification with JFET stage. The noise limit of 76 $\mu V/\sqrt{Hz}$ *and the theoretical performance of* 37 $\mu V/\sqrt{Hz}$ *are indicated by red and pink lines, respectively*

The measurement on the complete sensing circuit is indicating a noise ASD of $37\ \mu V/\sqrt{Hz}$ and the calculated value is $36{,}9\ \mu V/\sqrt{Hz}$ (Table D-2). This is now well below the limit (49%) of $76\ \mu V/\sqrt{Hz}$ and an improvement by factor 2.2 compared with the first version of the BB.

The measurement on the open TIA circuit is indicating a noise ASD of $9\ \mu V/\sqrt{Hz}$ and the calculated value is $8{,}9\ \mu V/\sqrt{Hz}$ (Table D-3). This is now an improvement by factor 7.8 compared with the first version of the BB.

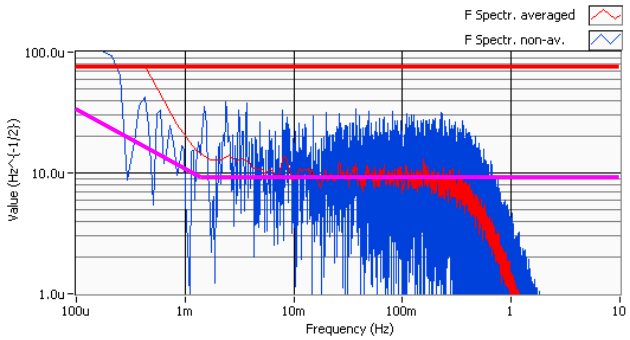

Figure 4-17 The noise of the sensing circuit with disconnected transformer bridge showing the dominating TIA noise. The noise limit of $76\ \mu V/\sqrt{Hz}$ and the theoretical performance of $9\ \mu V/\sqrt{Hz}$ are indicated by red and pink lines, respectively. At a low frequency of around 1 mHz the demodulator 1/f noise is dominating the TIA noise

The measurements also confirm the high *Q* of the transformer, which is around 409, measured either outside or in the bridge circuit.

It must be noted that an error occurred in the technical note written in 2006 during the description of the measurements [61]. Namely, the measurement with the disconnected transformer bridge with the result of $9\ \mu V/\sqrt{Hz}$ was performed on the differential TIA and not on a single TIA, as written in the note. This introduces a factor $\sqrt{2}$ difference in the noise.

With the successful modification and performance verification, a second BB based on the above-described achievements was built in 2010.

4.3.2 Sensing Noise at Non-Zero Test Mass Position

Maintaining the sensing noise performance at non-zero input capacitance is an additional challenge. Since the sensing noise is essentially multiplicative when larger input capacitance is measured (TM more off-center), a higher low frequency noise (fluctuation) is expected. There are several reasons for this, the straightforward one coming from the stability of the gain originating in the stability of the 100 kHz TM injection bias voltage (Figure 2-12). The stability of the parameters in the sensing bridge and the TM simulator stability can show up as the low frequency noise. The temperature fluctuation and related electronics sensitivity can mask the true performance and, last but not least, the grounding scheme in the electronics and the cable shielding between the TM and the electronics can also increase the low-frequency noise.

The test campaign is described in detail in [61]. An overview of different TM simulator designs is presented in 4.3.2.1, the injection stability verification in 4.3.2.2 and a summary of noise testing with the 10 µm and the 100 µm TM simulators in 4.3.2.3.

4.3.2.1 Test mass simulator

The sensing noise is verified at the end of the performance range (10 µm) and the end of the HR range. During the initial IS-FEE development, the HR range was twice smaller, i.e., 100 µm, this being the reason why the TM simulators were tuned for these two values. The TM

simulator must include two capacitors of roughly 1 pF like the nominal TM-electrode capacitance on the *x*-axis and must simulate the TM off-center position by tuning the difference between the capacitors by either 5,8 fF (10 µm) or 58 fF (100 µm). The simulator must have three terminals: one input for the injection bias voltage representing the TM body and two outputs representing two electrodes on each side of the TM. Simulating capacitors are thus placed between the common input terminal and each of the electrode terminals.

Figure 4-18 shows three initial TM simulators built inside small metal box. Since Mica capacitors are very stable, the first design was based on two 2,2 pF Mica capacitors in series. The second design was based on capacitors made from the printed circuit board (PCB) material (FR-4) and the third by using stable ceramic surface mount device (SMD) chip capacitors (NPO grade), i.e., three 3,3 pF capacitors in series. In all designs the electrode terminals (BNC coaxial connectors) must have isolated shield from the box. This prevents ground loops, i.e., return currents flowing over the cable shield back to the sensing bridge. The shield of the injection terminal can be connected to the box, but depending on how the grounding is made in electronics, it can have a positive or negative effect on the low frequency noise.

In all three initial designs, the small box appeared to cause the large stray capacitance, which was the reason for the large sensing noise at low frequency. Depending on the grounding, the ground current fluctuation was transferred via the large stray capacitance to the internal capacitors (too close to the box walls) causing the noise. In addition, the PCB capacitors had very high losses, which modified the phase of the injection bias on the output terminals, making this simulator unusable.

The single 2,2 pF Mica capacitor has the quality factor Q of only 240-290 and has detrimental influence on the sensing bridge (its white noise) with Q = 400. Larger Mica capacitors (e.g., 330 pF) have much larger Q but cannot be used for this application. Best performance has been achieved with the SMD chip capacitors mounted on a small PCB. Three SMD capacitors in series have Q of 400. The capacitance tuning was performed by bending the connecting wires.

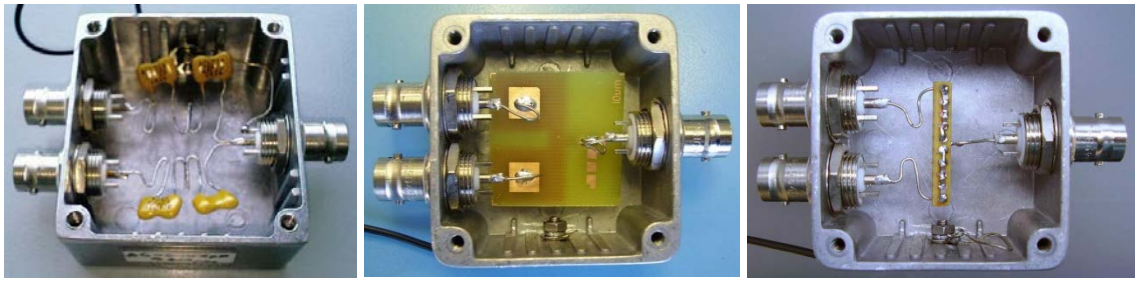

Figure 4-18 The line of poor TM simulator designs in a small box: with Mica capacitors (left), PCB capacitors (middle) and SMD capacitors (right)

The use of the large box (Figure 4-19) immediately improved the sensing noise due to reduced stray capacitance. All designs were based on SMD capacitors, the latest with the improved mechanical stability as a result of mounting capacitors on the board attached via Teflon spacers to the box.

Figure 4-19 The line of successful TM simulator designs in a large box, all based on SMD capacitors. First simulator design (left), the dual 10 µm and 100 µm TM simulator (middle) and the latest design (right)

Details on how the capacitance can be effectively tuned are shown in Figure 4-20. The wires or copper sheets create an air capacitor that is added to the chip capacitors. With these TM simulators the performance was successfully tested up to 1 mHz. For LISA a more stable design is needed. This work has already started but is not part of this dissertation.

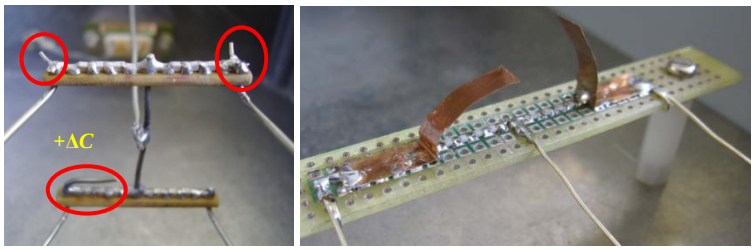

Figure 4-20The femto Farad capacitance tuning. The position of small wires at the end of series of three SMD capacitors changes the capacitance in each simulator arm and bending a wire over capacitors generates a large positive capacitance change (left). The same effect is achieved by bending copper sheets over each TM simulator arm (right)

4.3.2.2 TM injection voltage stability

The TM injection stability was verified using the same demodulator of one sensing channel with the disconnected front-end AC circuit. The nominal TM amplitude level of 0,6 V peak was generated using the control board (4.4.2) and an external stable voltage source (Yokogawa 7651 calibrator) connected to it. The voltage source was used to set the DC level corresponding to the desired waveform amplitude.

During the breadboarding the external voltage source was used instead of an internal voltage reference to simplify the hardware and adopt the concept suggested by the end-user (University of Trento). This does not mean that the voltage reference is not important or that it is not a challenging design, certainly not for LISA and its 0,1 mHz bandwidth.

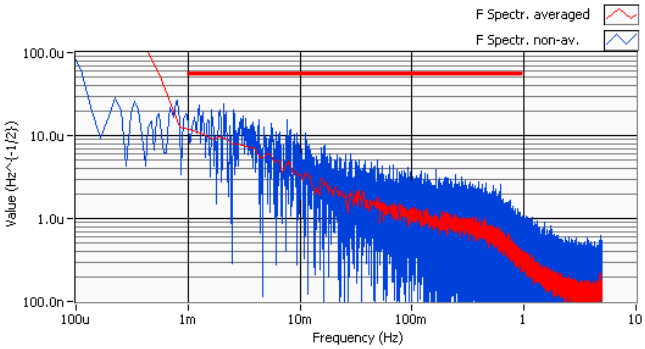

Figure 4-21 The amplitude stability of the 100 kHz TM injection waveform with the corresponding $50\,ppm/\sqrt{Hz} = 38\,\mu V/\sqrt{Hz}$ *stability (noise) limit*

The test result shown in Figure 4-21 is satisfactory up to 1 mHz. The low frequency fluctuation is actually dominated by the test demodulator, which had the noise roughly $12\,\mu V/\sqrt{Hz}$ at 1 mHz (see Figure 4-17). Since the demodulator has a gain of 1,28, the DC output is 0,768 V, for which the $50\,ppm/\sqrt{Hz}$ requirement is equal to $38\,\mu V/\sqrt{Hz}$. It can be concluded that the injection voltage stability is better than actually measured and is thus more than adequate for further testing.

4.3.2.3 Sensing noise measurements

The sensing noise results [61] shown in Figure 4-22 are for the TM simulator made of SMD chip capacitors (Figure 4-18). The noise limit for the TM displacement of $\leq$ 10 µm is $1\,aF/\sqrt{Hz}$, which is on the first BB equivalent to the $76\,\mu V/\sqrt{Hz}$ noise at the sensing output. This is the theoretical value based on the nominal sensing gain. It was found later that the effective gain is slightly lower, so the limit was reduced accordingly to $70\,\mu V/\sqrt{Hz}$, as shown by the red line on the noise plots. In LTP the noise is specified between 1 mHz and 30 mHz, this being the reason why the limit is sometimes shown only in this bandwidth.

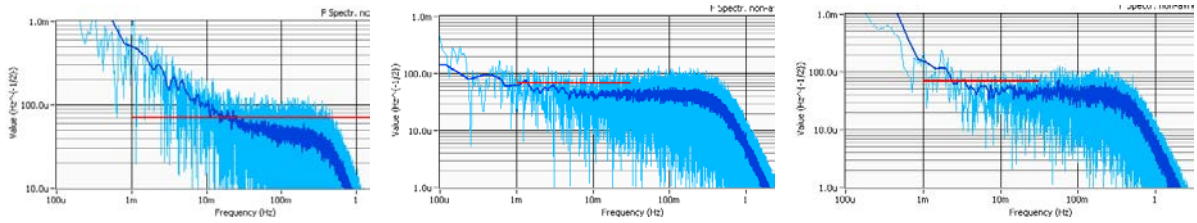

Figure 4-22 The sensing noise with the 10 µm TM simulator inside the small metal box: injection shield disconnected from the box (left), same as previous but with simulator tuned for ≈ 0 µm (middle) and with a nominal 10 µm TM simulator, but with shield connected to the box (right)

While the white noise floor remains the same, measured either without the TM simulator or with switched off injection bias, the low frequency noise is very large with this TM simulator. When the simulator is tuned to zero the noise automatically decreases to almost the white noise level (middle plot), confirming the statement that the noise is multiplicative with the TM off-center position. When the injection bias shield was connected to the TM simulator, box the noise decreased considerably, as shown on the right plot.

The results of measurements with the 100 µm TM simulator are shown in Figure 4-23. Again the simulator inside the small box generated enormous noise. Note that according to Figure 2-12, the noise limit for the 100 µm TM displacement is much larger, i.e., $7{,}6\,aF/\sqrt{Hz} = 530\,\mu V/\sqrt{Hz}$. Nevertheless, both the 10 µm and 100 µm limits are shown on the plots. With the TM simulator in the large box (Figure 4-19), the sensing noise is well below the limit and almost satisfies the 10 µm limit.

This means that the excess noise at 10 µm TM displacement does not have its origin in the injection bias instability since larger noise would appear at a larger displacement. It is rather related to the grounding scheme and the temperature fluctuation effects. The temperature fluctuation (noise) was continuously measured in the laboratory and was approximatelly the same at low frequency, irrespective of whether the electronics and the TM simulator were isolated thermally by the styrofoam box or left open. The PSD of the thermal noise has the $1/f^2$ shape ($1/f$ for ASD) and has a level of $40 - 50\,mK/\sqrt{Hz}$ at 1mHz ($0{,}4 - 0{,}5\,K/\sqrt{Hz}$ at 0.1 mHz).

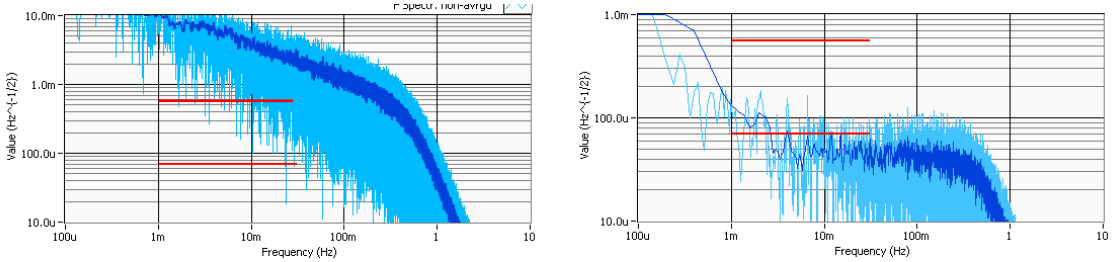

Figure 4-23 The sensing noise with the 100 µm TM simulator in a small box (left) and large box (right). The noise limits for the 100 µm and 10 µm measurement ranges are shown by upper and lower red lines, respectively

The grounding scheme and the EMI protection, producing the best noise results, is shown in Figure 4-24.

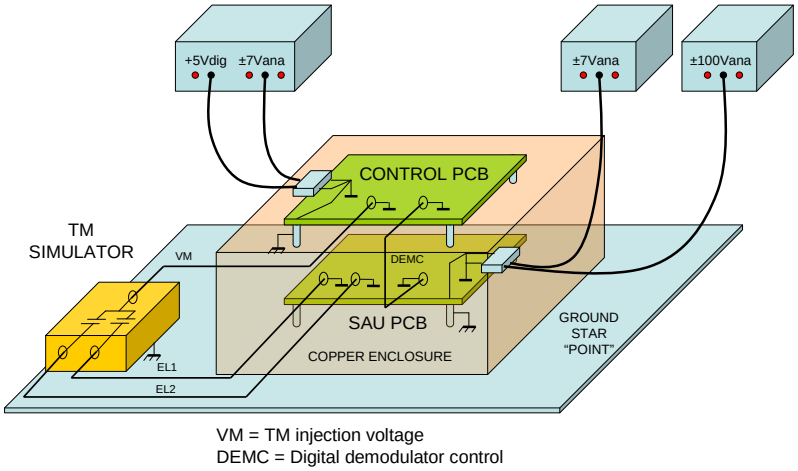

Figure 4-24 The grounding scheme and the EMI protection of the first BB with the sensing and atuation (SAU) board inside the copper enclosure and the control board on top

The main chassis-ground star point is the metal plate on which the SAU PCB is mounted. The SAU PCB receives power from two power supplies that have isolated grounds. These grounds are connected together on the PCB near the power supply connector. The common PCB ground plane is connected to the metal mounting spacers, which are then making a connection with the chassis.

The SAU PCB is covered with the copper enclosure against EMI. The Control PCB is mounted on top of the enclosure and is generating an analog injection bias signal for the TM (VM) and the digital TTL control signal for the demodulator of the SAU PCB (DEMC). Control PCB receives digital and analog grounds from isolated power supplies. These two grounds are connected to corresponding ground planes on the control PCB and are connected in one point on the board. The common ground point is connected to the (one) metal mounting spacer, which makes connection to the chassis via copper enclosure (mounting spacers are actually extended from the bottom PCB).

The shield of the DEMC signal connects digital ground from the control PCB to the analog ground of the SAU PCB. This is not convenient (potential ground loop), but was necessary. If one side of the shield were left open, the 100 kHz DEMC TTL signal would generate a large offset in sensing output. This is because the extremely sensitive front-end, tuned to 100 kHz, is not separately enclosed and thus the pick-up from this DEMC cable would be large. This was improved in the second BB.

The TM simulator has all 3 coaxial cable shields isolated from its box and the box itself is connected with the chassis (bottom plate). Note that the large noise improvement seen on small box simulators by connecting the injection bias shield to the box had a very small, but also positive, effect when the simulator was made in the large box.

The final sensing noise result with a 10 µm TM simulator is shown in Figure 4-25. The incompliance of the first BB at 1 mHz is between 35-40% and the sensing performance is compliant down to 2 mHz. Since the noise ASD below 1 mHz has the 1/f shape, it must be dominated by the thermal effects. The noise result of the second BB has a slightly better low-frequency noise performance, but the white noise floor grew in size due to the planar transformer design with a much smaller quality factor.

It is obvious that some more work has to be done to improve the sensing performance down to LISA 0,1 mHz frequency.

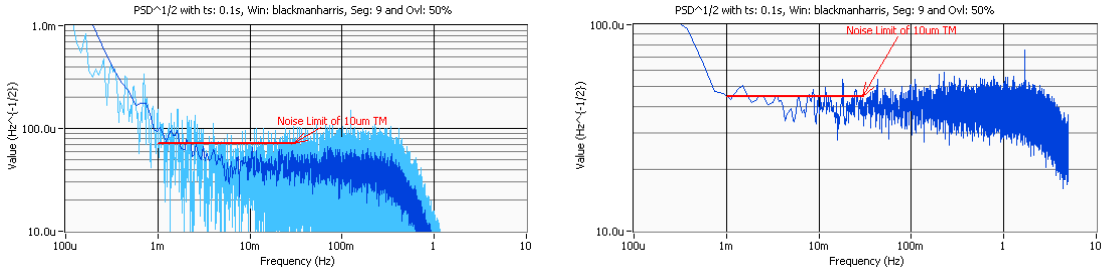

Figure 4-25 The noise result of the first (left) and the second (right) BB for the 10 µm TM displacement. Note different gains and white noise levels w.r.t. limit in two BB designs

4.4 Actuation Channel Design and Measurements

There are 12 actuation channels in the IS-FEE, each one dedicated to one TM electrode. Each channel receives the digital actuation amplitude on its input, which is then converted into an analog voltage, amplified and filtered. The output is applied on the TM electrode via the sensing transformer primary winding, which is a short circuit for the low frequency actuation waveforms.

The digital logic, i.e., the PID and PWM controllers, analyzed in 3.4.1 and 3.4.2, which are suggested to enhance the noise and / or DAC resolution, were not implemented in the BB. Instead, the analog circuitry was directly driven by the external DAC cards in PC or by external stable voltage sources, thus providing the required actuation amplitudes already in the analog form. The actuation waveform generators were realized on the separate control board in two versions according to the pulsed and the sine actuation schemes. The following sections describe in more detail the actuation architecture and the results of the test campaign.

4.4.1 Actuation Drive Electronics

The drive voltage amplifier (DVA) resides on the sensing and actuation (SAU) board and its design in both BBs followed the suggested schematic shown in Figure 3-13. Since at the time of the BB development the maximum required actuation voltages were 100 V DC, suitable for the pulsed actuation scheme, the realized BB hardware design is somewhat different from this schematic. The changes can be summarized as follows:

- Since the maximum voltage was 100 V, the DVA power supply was ±110 V
- Different transistors were used (NPN 2N3439 and PNP 2N5416) since a lower voltage rating of at least 350 V was acceptable
- The gain was adapted for a different input level (±5 V) and output level (±20 V in HR mode and ±100 V in WR mode)

- The first BB design has the second order output low-pass filter and the second BB the third order, both having equal -3 dB corner frequencies. The latter was implemented to additionally suppress the 100 kHz residual signal in order to reduce the sensing noise
- Different auto-zero amplifier was used (LTC1051) because at that time the suggested space qualified auto-zero amplifier (AD8629) did not exist
- The larger analog power supply level was used (±7,5 V), suitable for the used parts

The DVA circuits are shown in the middle part of the SAU board in Figure 4-3.

4.4.2 Actuation Waveform Generator

The waveform generators are realized on the control board and are represented by the block diagrams shown in Figure 4-26 and Figure 4-27. They refer to the first BB with the pulsed actuation scheme and the second BB with the sine actuation scheme, respectively.

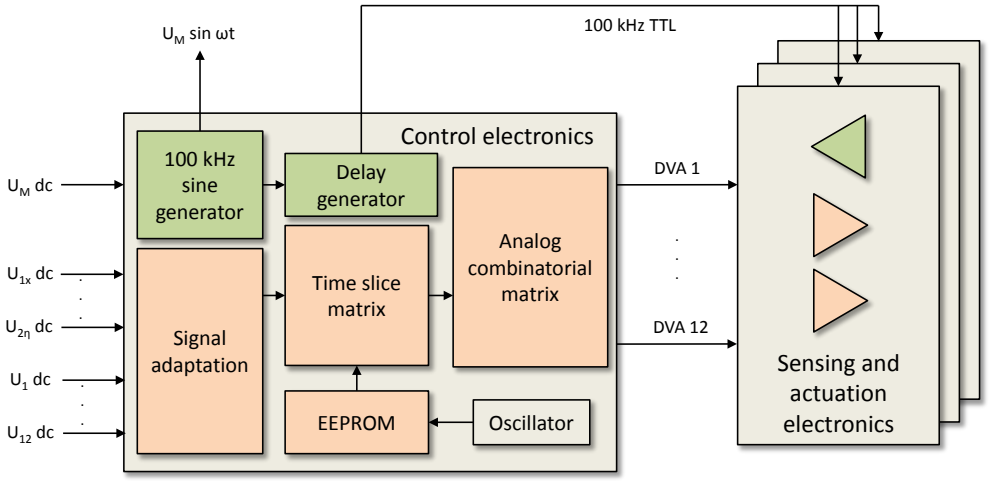

Figure 4-26 The block diagram of the control board of the first BB with the pulsed waveform generator. Blocks related to the sensing function are shown in green

In the pulsed actuation waveform scheme (Figure 4-26), the pulses resembling the sine and cosine signals (Figure 3-3) are generated with analog switches, which are ON / OFF controlled by the time slice matrix block. The repetitive time event generator is stored in the electrically erasable programmable read-only memory (EEPROM), which has an oscillator for the time base.

The input signals are DC voltage levels representing 12 AC peak voltages (forces and torques) and 12 DC voltages that can be added to the AC waveforms as an offset. After the adaptation of the ±10 V input voltages into maximum ±5 V range, the force and torque voltages are switched ON / OFF at the right moment and combined with the DC offsets in the analog combinatorial block. The final actuation voltages are output to the DVAs located on three SAU boards.

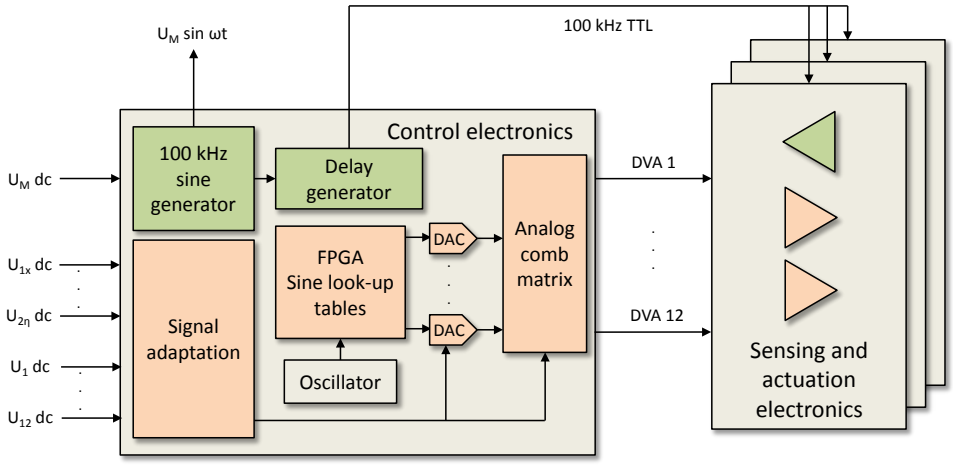

Figure 4-27 The block diagram of the control board of the second BB with the sine waveform generator

In the sine waveform generator (Figure 4-27) the FPGA replaces the EEPROM to store the sine waveform samples at correct frequencies for each degree of freedom (3.11), (3.12), (3.13). Since the same 16 MHz oscillator was used for the pulsed and the sine waveform generator, the exact frequencies suggested on the project could not be realized and were reduced by 7,4% on the BB (55,55 Hz instead of 60Hz and 250 Hz instead of 270 Hz); this had no influence on the performance. The FPGA continuously updates each multiplying type DAC with the waveform samples for the unity amplitude level.

Each input analog voltage (except offset voltages) is applied to the DAC's voltage reference input to scale the DAC output to the reference voltage level. The zero input level will thus generate a waveform with zero amplitude. The correct sign and combination of different AC voltages and DC offsets is finally made in the analog combinatorial block.

In both versions of the control board, a TM injection bias waveform of 100 kHz is generated with the amplitude level according to the input U_M DC level. The schematic follows, in principle, the design shown in Figure 2-19. To control the sensing demodulators, the board generates a synchronous digital TTL signal that can be phase-shifted (lead or lag) according to the external digital control word. Similarly, this word controls the HR and WR mode switching of the IS-FEE. The schematics of both versions of the control board (Figure 4-28) are not shown because they are quite complex and it is in any case the auxiliary electronics that are needed to operate the more challenging SAU board.

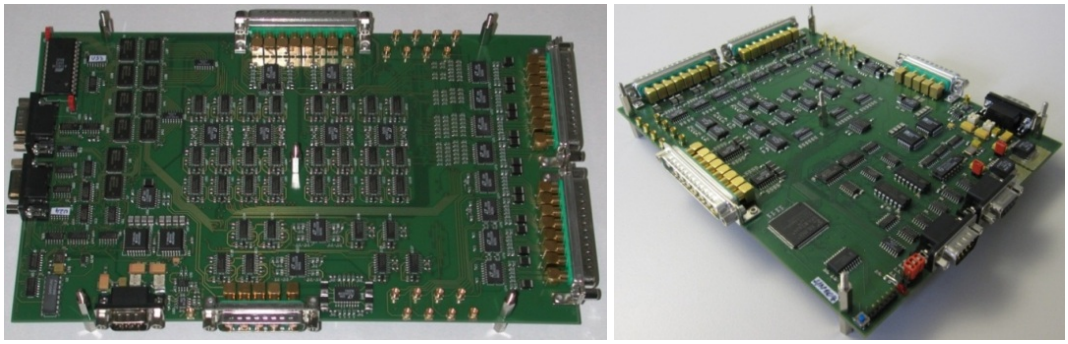

Figure 4-28 The first (left) and the second (right) version of the control board

The examples of the pulsed and sine waveforms are shown in Figure 4-29 and Figure 4-30, respectively.

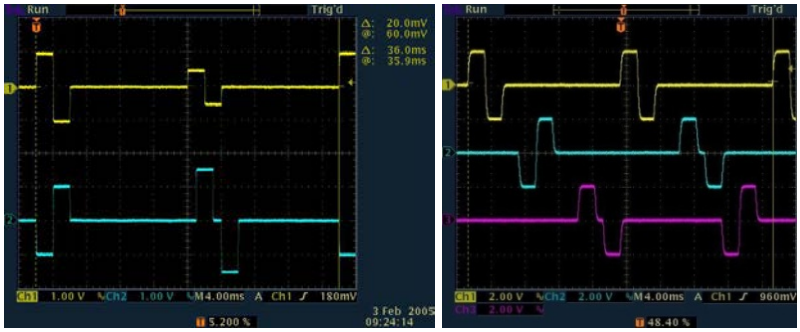

Figure 4-29 Pulsed actuation waveforms in the 36 ms actuation cycle at the output of the control board (left) and filtered on DVA output (right). The time slicing of different degrees of freedom (for three SAU boards) is shown in the right figure

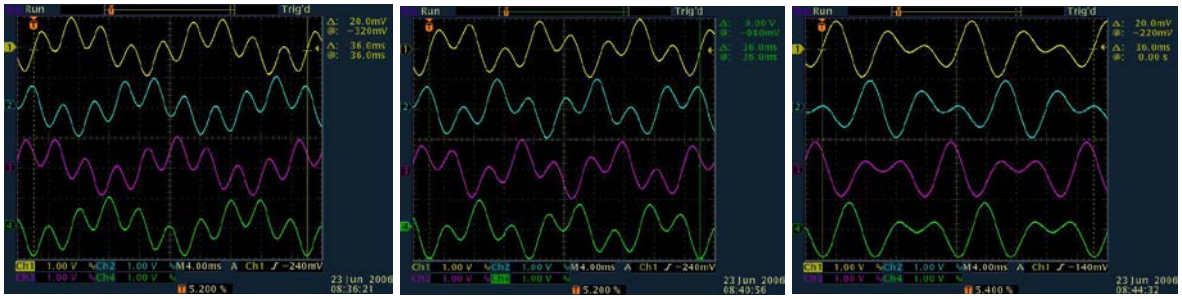

Figure 4-30 Composite sine actuation waveforms in the 36 ms actuation cycle for electrodes EL1 to EL4 at 55,6 Hz and 250 Hz (left), electrodes EL5 to EL8 at 83,3 Hz and 222,2 Hz (middle) and electrodes EL9 to EL12 with 111,1 Hz and 166,7 Hz (right)

4.4.3 Actuation DC Noise

The actuation DC performance of the first BB was successfully verified by measurements at zero and non-zero output voltage, as shown in Figure 4-31 and Figure 4-32, respectively.

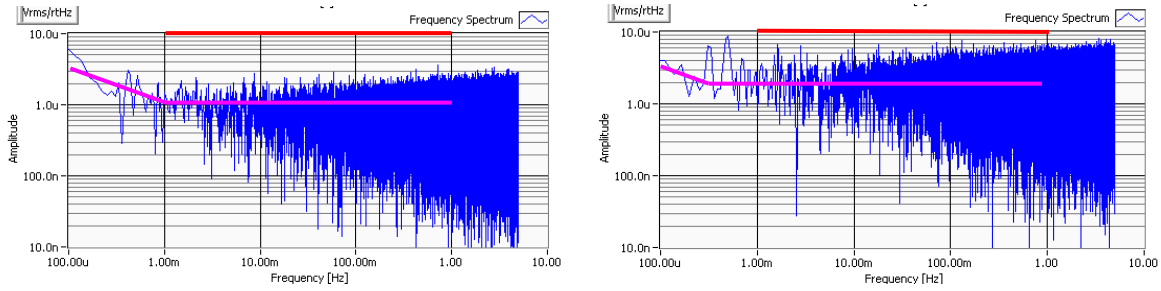

Figure 4-31 The actuation noise of the first BB with shorted DVA input (left) and shorted control board input (right). The noise limit of $10\,\mu V/\sqrt{Hz}$ *is indicated by the red line. Since the noise ASD is not averaged, a pink line is indicating the achieved noise performance of* $1\,\mu V/\sqrt{Hz}$ *and* $2\,\mu V/\sqrt{Hz}$ *, respectively. The noise at 0.1 mHz is* $3\,\mu V/\sqrt{Hz}$

The noise enlargement on the right plot is due to additional noise of the control board. Note that the DVA of the SAU board and the electronics of the control board are designed with the auto-zero amplifiers, which reduce the $1/f$ noise to the level small enough to appear only below 1 mHz.

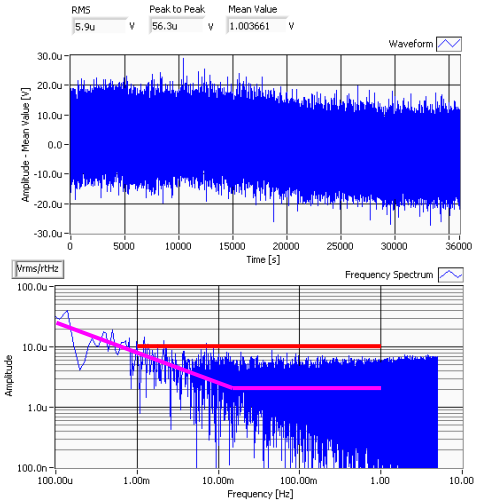

Figure 4-32 The actuation time domain plot (top) and the noise of the first BB at non-zero output. The Yokogawa 7651 calibrator at 0,5 V DC output was used to generate the DVA output of 1 V DC. The limit and the achieved performance are indicated by the red and pink lines, respectively

Since the control board is rated for the ±10 V input range and the actuation output in the HR mode for the ±20 V range, the effective gain of IS-FEE is two. In fact, the control board first attenuates the input by factor two and then the DVA amplifies the control board output by factor four in HR mode. Although the noise is satisfied at 1 V output (Figure 4-32), the effects of the gain instability of the instrumentation, in particular the voltage calibrator, introduce the 1/*f* noise. This is discussed in more detail in the next section.

4.4.4 Actuation Stability

The verification of the actuation stability requirement ($2\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$) is the most difficult because it can be easily masked by the instruments' poor performance at low frequency and, in particular, in a high output range. The IS-FEE performance related to this requirement is affected by two main fluctuating sources: the gain instability of the actuation chain, i.e., mostly by DVA and less by the electronics of the control board, and the gain instability of the input voltage source used to set the required output level. The latter would be the voltage reference chip and the analog output circuit of the actuation DAC in case the BB would represent identically the IS-FEE. In both versions of the IS-FEE BB, the voltage reference and the actuation DAC were replaced by the external voltage source Yokogawa 7651 and later by the more stable Krohn-Hite 511. Therefore, the BB is not complete in this respect but allows verifying the gain instability of the DVA and the control electronics. The gain stability of the instrumentation is also shown for the reference and its influence is discussed with respect to the achieved performance.

Many measurements have been conducted at different output voltages and in different thermal environments. The best performance has been achieved with the Styrofoam insulation of the instruments and electronics, as shown in Figure 4-33.

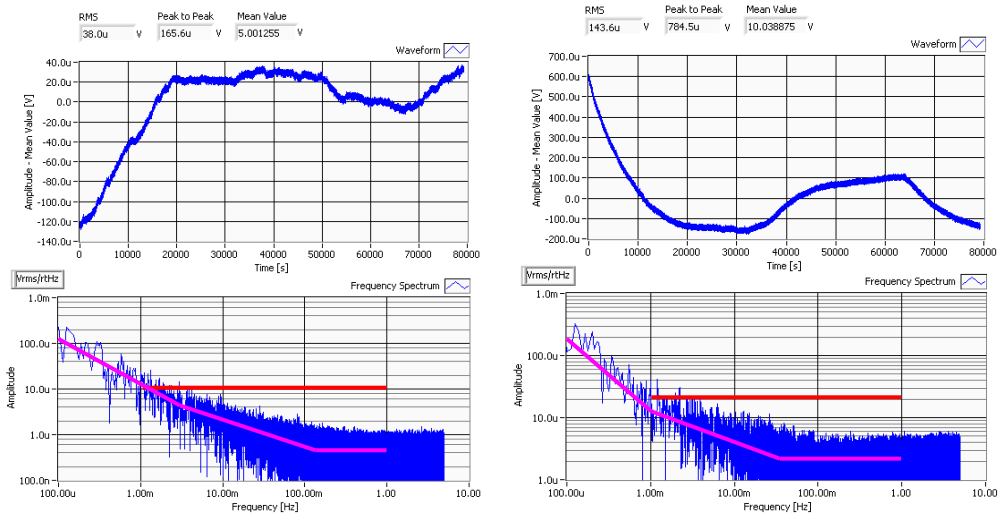

Figure 4-33 The actuation stability measurement of the Krohn-Hite 511 calibrator at 5 V DC (left) and the DVA output at 10 V DC (right). Upper plots show the time series of 22 h long measurement. Limits are adapted for 5 V and 10 V levels

The gain fluctuation in the voltage calibrator and the digital multimeter at 5 V output (DMM) is barely compliant with the $2\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ requirement at 1 mHz. From the noise shape at 1 mHz and below ($1/f$ in ASD) it can be concluded that the instruments' noise is dominated by the thermal effects. At higher frequencies the standard pink noise ($1/\sqrt{f}$ in ASD) dominates. The same is reflected on the actuation output, just scaled to the 10 V output and with additional white noise of the electronics.

One can conclude from the above plots that the IS-FEE gain fluctuation is much smaller and that the result, still compliant down to 1 mHz, is dominated by the instrument fluctuation. The time series plots show good correlation of the actuation output with the calibrator output voltage.

The differential measurement (Figure 4-34) on the second BB, between two channels outputting 5 V DC, confirms that the IS-FEE BB electronics gain fluctuation at non-zero level is smaller than the input voltage calibrator gain fluctuation. Since the measurement is differential, the white noise (> 0,1 Hz) is also increased from roughly $2\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ on previous graphs to $3\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ (factor $\sqrt{2}$).

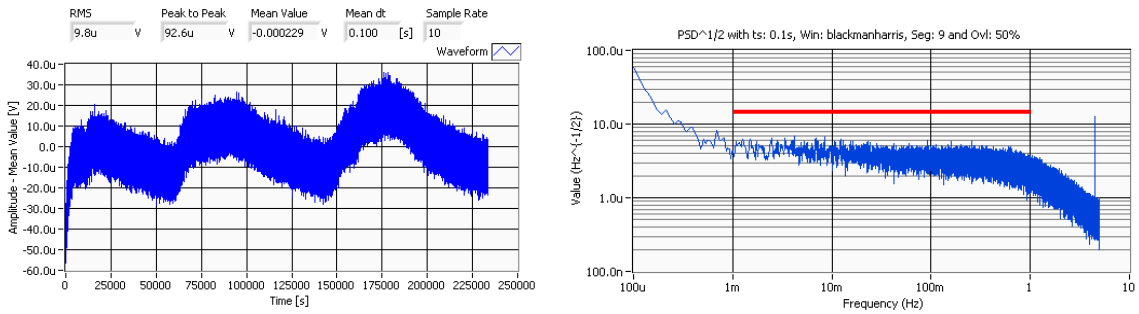

Figure 4-34 The 2,7 days long differential measurement of two actuation outputs at 5 V DC from the second BB. The stability of the common-mode external voltage source is with this measurement rejected and the result thus shows the differential gain instability of the actuation circuits (DVA and control board). Because of differential measurement, the noise limit is increased from $10\,\mu V/\sqrt{Hz}$ *(*$2\,ppmV/\sqrt{Hz}$*) to* $14\,\mu V/\sqrt{Hz}$*. An additional 1 Hz low-pass filter has been used before the DMM to reduce aliasing effects due to the high-frequency content at the DAC update frequency*

4.4.5 Actuation Crosstalk to Sensing Circuit

In the history of the IS-FEE development one can find two terms used for the unwanted sensing output due to application of actuation signals. Sometimes this is called cross coupling and sometimes crosstalk. The correct name should be crosstalk since cross coupling is more used for actuation to actuation and sensing to sensing influence where different degrees of freedom mix with each other. This section deals with two different types of cross talking:

- The saturation of the sensing circuit due to the application of actuation signals at a high slew rate
- The change of the sensing offset when either DC or AC actuation signals are applied

In both cases the sensing output changes either transiently or has a constant shift. The crosstalk occurs at the sensing transformer bridge, which is the common point where the sensitive sensing currents and actuation voltages meet. Such sensing output deviation is generally not a problem if it is well understood, can be modeled and compensated by post processing of sensing data.

The saturation effects in the form of transients depend on the type of actuation waveform (pulsed or sinusoidal) and can be eliminated by proper distribution of the sensing gain, reduction of the DVA bandwidth, high-pass filtering of actuation frequencies and by sequential actuation with a lower slew rate [67], [68], [69].

The other type of crosstalk can be particularly troublesome during the measurement of the accumulated charge on the TM. This is normally performed by applying sinusoidal voltages at low frequency (dither) and by observing possible TM motion. If this motion becomes corrupted by the crosstalk at the frequency of the dither, which would be the case in presence of large crosstalk, wrong charge would be detected. If the effect is also non-linear and / or difficult to model, it cannot be compensated. Detailed investigation on both BBs have been conducted to find the source of such a crosstalk [70], including some recent findings [71], which are believed to be the true cause for the crosstalk.

4.4.5.1 Crosstalk due to the slew rate

With the pulsed waveform scheme the maximum levels are 20 V in the HR mode and 100 V in the WR mode. With the sinusoidal waveform scheme in the HR mode, maximum level occurs for z-axis composite waveform as the sum of to 9,1 V peak and 3,5 V peak sine waveforms at 120 Hz and 180 Hz, respectively. At the time the slew rate was investigated the pulsed actuation scheme was always applicable to the WR mode, i.e., no sinusoidal option for the WR mode. Afterwards, the actuation with maximum 140 V at a single frequency of 120 Hz for all degrees of freedom was selected for the WR mode.

The investigation with the pulsed waveforms [67] showed by simulation and measurement that the 20 V HR mode steps with a nominal DVA bandwidth of 1,2 kHz generate an actuation voltage slew rate of 80 V/ms, which saturates the main sensing AC amplifier due to very asymmetric differential TIA output. This happens because the step transients easily pass through the capacitive coupling of the transformer, then through the decoupling capacitors and appear at the TIA input. This causes the change of the TIA DC output and saturation of the main amplifier, as shown in captured oscilloscope screens of Figure 4-35.

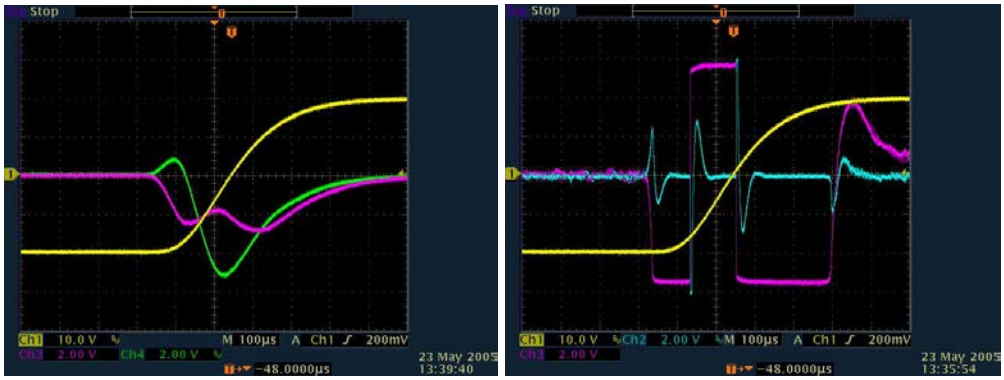

Figure 4-35 The worst case slew rate condition when the actuation waveform is stepping from -20 V to +20 V (yellow trace) and causes asymmetric offset shift of two TIAs up to 5 V (left plot, green and pink traces). This subsequently causes saturation of the main amplifier and transients after the band-pass filter (right plot, pink and blue traces, respectively)

The 1,6 V stepping actuation is already saturating the amplifier. The measurements with 2 V steps generate finally a maximum 250 nm sensing offset shift, as shown in Figure 4-36.

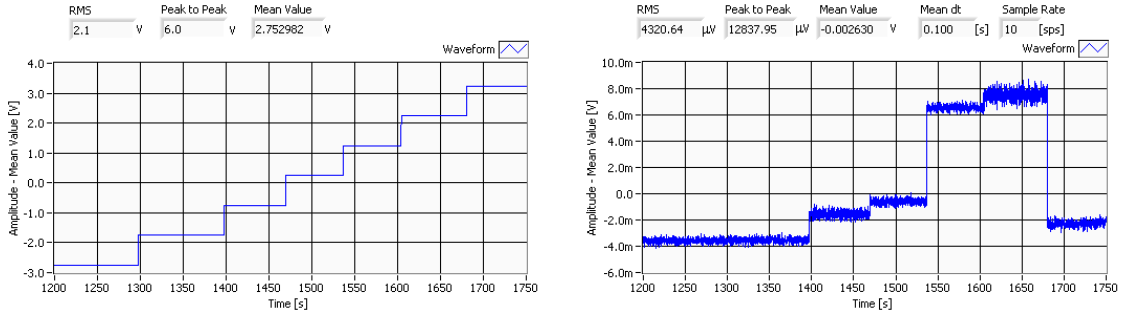

Figure 4-36 The control board input voltage stepping of 1 V produces the actuation steps of 2 V, which generate non-linear effects on the sensing demodulator and maximum offset shift of roughly 12 mV = 250 nm

It has been simulated that the slew rate must not exceed 20 V/ms, i.e., a reduction of 4 times, to prevent the saturation. This can be achieved by reducing the DVA bandwidth four times or by redistributing the sensing gain between the TIA, amplifier, and filters. In the detailed investigation of the proposed solutions, the transformer and the TIA models were successfully generated to produce the same responses (Figure 4-37) as the measured ones [68].

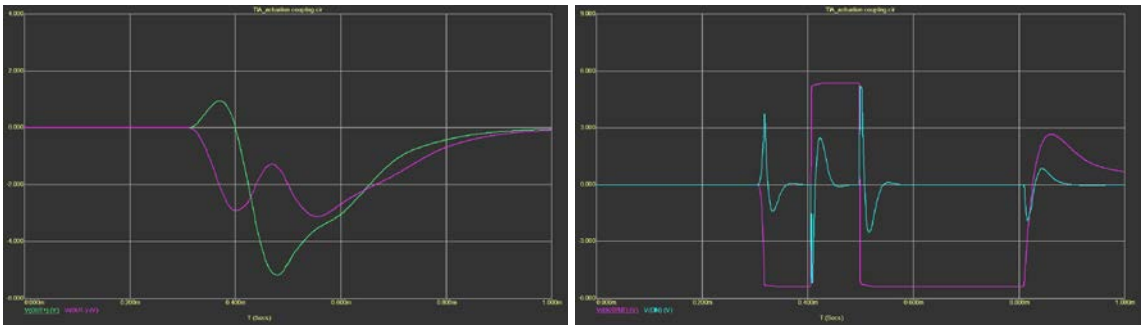

Figure 4-37 The simulated transients with the ±20 V stepping, TIA on the left and amplifier and the band-pass filter on the right. The vertical axis grid spacing is 2 V and horizontal 200 µs. The traces are to be compared to Figure 4-35

Finally a combination of possible changes is suggested with respect to the pulsed waveforms, since large reduction of the DVA bandwidth, as a single solution, is not acceptable. This is because it causes incompliance in the waveform orthogonality (actuation independency between different degrees of freedom) [67]. Therefore, the DVA bandwidth will only slightly reduce from 1,2 kHz to 0,9 kHz.

In the WR mode the main amplifier gain is reduced, which assures the saturation free performance up to 32 V stepping. Beyond this level the TIAs saturate and therefore an operational constraint has been suggested, i.e., the maximum actuation accomplished in three steps. Otherwise, one has to reduce the TIA gain.

The final solution for the gain distribution suitable to pulsed waveforms is as follows [69]:

- Reduce TIA gain 10 times (C_{FB} = 33 pF)
- Reduce amplifier gain twice or 4 times depending if FSR = ±200 µm or ±100 µm, respectively (G = 32)
- Enlarge the band-pass filter gain 5 times (G = 6,65)
- Enlarge the low-pass filter gain (after demodulator) ~3 times (G = 6,3)

The drawback of this modification is that the sensing offset limit becomes equivalent to few mV and thus more difficult to be achieved with standard op-amps.

The low duty cycle in the pulsed actuation concept, i.e., the need for larger voltages to generate necessary forces as well as the modifications needed to reduce the crosstalk, were the reasons why the pulsed waveforms were finally abandoned in the project.

The sinusoidal actuation with a maximum composite waveform level of 12,6 V in the HR mode also produced similar crosstalk. It was removed by five times reduction of the low-pass filtering in the control board, i.e., to 2,4 kHz and by the DVA bandwidth reduction to 0,9 kHz [68]. The problem is not in the sine waveform slope, but in the DAC update frequency of 8 kHz used to generate the sine waveform. Even after DVA filtering the residual 8 kHz signals (though not visible) were able to saturate the amplifier (Figure 4-38). The saturation in the HR mode can be easily removed by the bandwidth reduction on the control board.

The similar sensing gain redistribution for the WR mode with the pulsed waveforms was suggested [69], but as it has already been mentioned, the sinusoidal actuation also replaced the pulsed waveforms in the WR mode and the modification was no longer necessary.

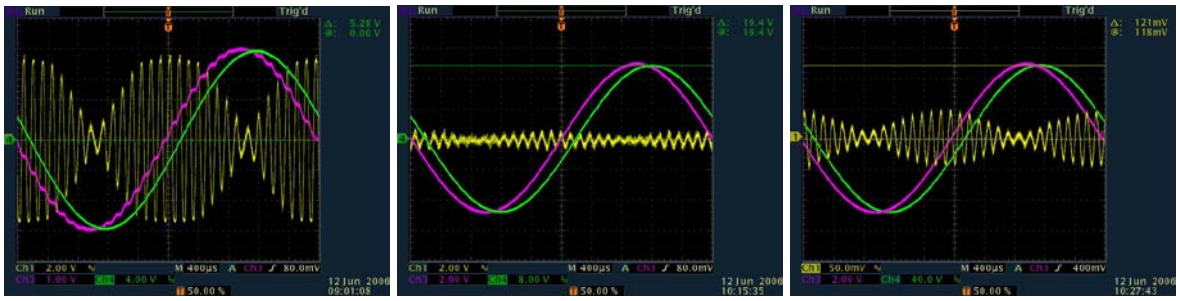

Figure 4-38 The DAC steps in the control board output at 8 kHz (pink trace), not visible in the DVA output of 12 V peak (green trace), cause saturation of the main sensing amplifier (yellow trace) when the control board bandwidth is large (left) and no saturation at five times reduced bandwidth and even enlarged actuation to 20 V peak (middle). The same modification ensures no saturation in the WR mode at 100 V peak actuation (right)

An additional solution to reduce the sinusoidal actuation crosstalk is to enlarge the corner frequency of the TIA high-pass filter consisting of the feedback resistance (R_{FB} = 10 MΩ) and the forward decoupling capacitor (C_D = 10 nF), Figure 4-7. By reducing the resistance to

5,6 MΩ the high-pass filter will attenuate the actuation transients more. Further reduction of the feedback resistor is not suggested as it would enlarge the sensing noise. The real part of Z_{FB} is getting larger with smaller R_{FB}, which increases the thermal noise (Table 4-4).

4.4.5.2 Crosstalk due to the offset shift

During the test campaign with the first BB, a shift of the sensing output was observed, which was correlated with the actuation dither, the low frequency DC variation [70]. The sensing output fluctuation is at the frequency of the dither and is proportional to its amplitude. An example of such a crosstalk is shown in Figure 4-39.

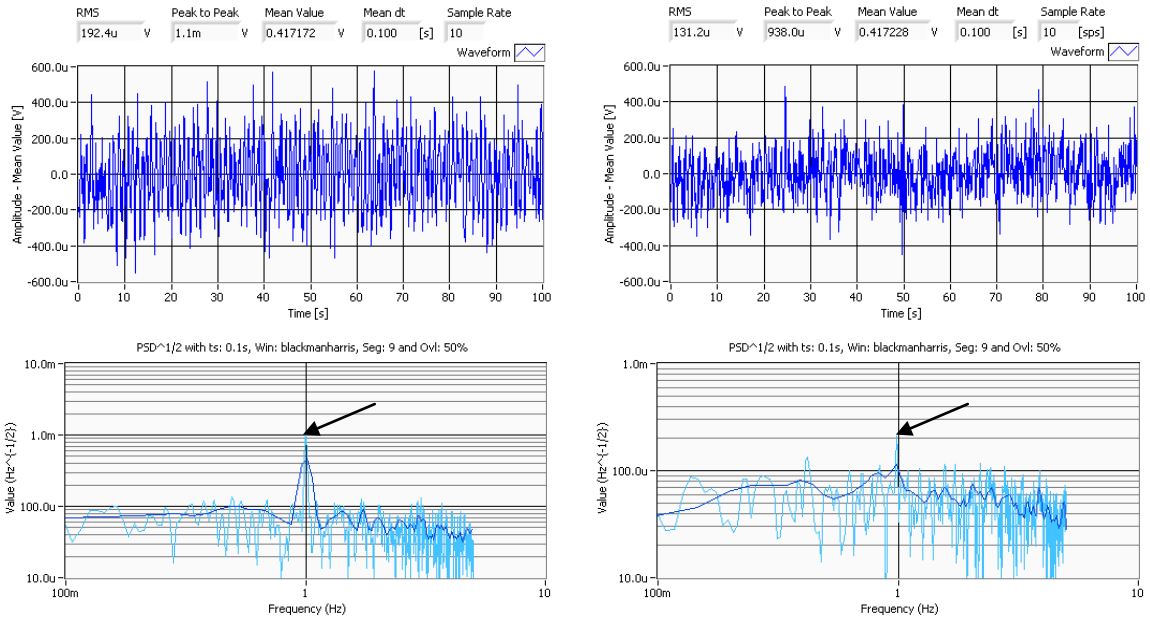

Figure 4-39 The sensing crosstalk due to the 5 V peak, 1 Hz actuation dither signal (left) and 1 V peak, 1 Hz actuation dither signal (right). The crosstalk peak in the sensing spectrum, indicated by the arrow, also decreases five times. The 1 Hz crosstalk in the time series (upper graphs) is clearly visible

The crosstalk was also present when the DC actuation was applied as a step, which is clearly visible in Figure 4-40 as a change in the sensing output and increased noise at low frequency.

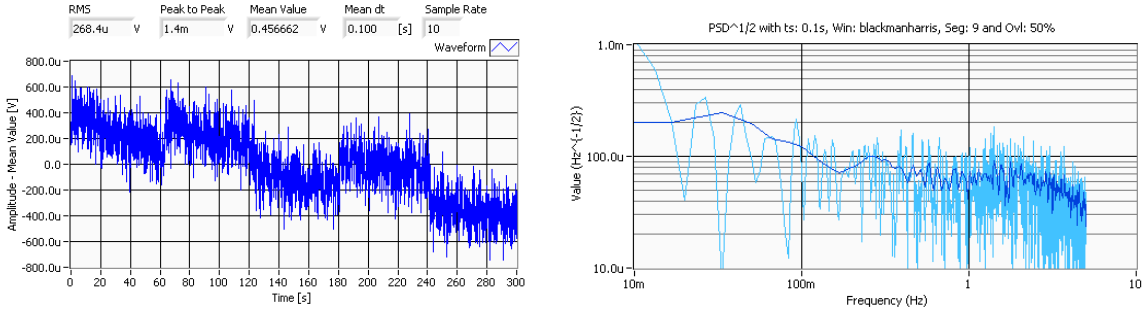

Figure 4-40 The crosstalk due to ON / OFF application of the 5 V DC actuation every 60 s

It has been confirmed by the debugging campaign that the crosstalk is not induced by radiation and that it is not present in the sidebands around the 100 kHz at the demodulator input [70]. Therefore, the investigation turned towards the board layout problem and the grounding issues. To investigate this, a SAU board was modified such that the actuation circuits, normally associated to the A sensing channel, were connected to the B channel and vice versa. This is shown in Figure 4-41, where the last passive actuation filters were

reconnected by yellow wires. This was done because of a large ground plane separation in the middle of the board (between A and B channels) that would with this modification separate some of the actuation return currents from the associated sensitive sensing circuit.

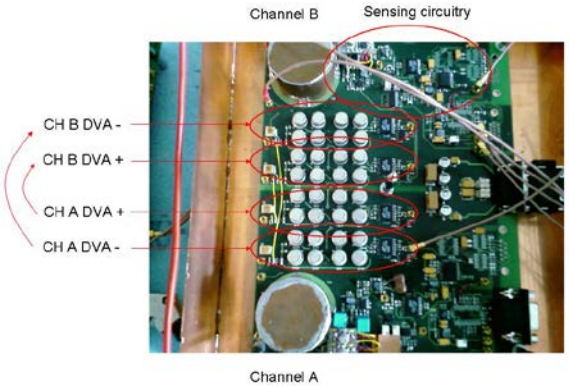

Figure 4-41 The modification of the first BB by exchanging the DVAs between A and B channels (DVAs of channel A connected to the sensing circuit B and vice versa)

The crosstalk from the step-like actuation disappeared in time domain and the low frequency noise decreased, as shown in Figure 4-42.

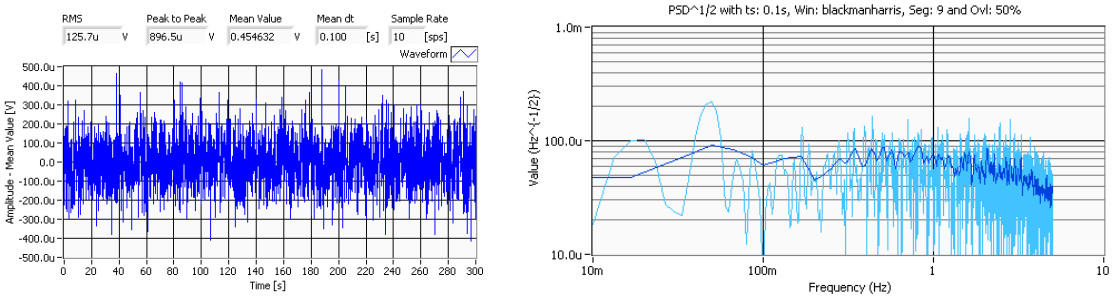

Figure 4-42 No crosstalk due to ON / OFF application of the 5 V DC actuation every 60 s

The crosstalk was no longer visible with a 5 V dither but could be observed with a ten times exaggerated dither level (Figure 4-43). Since during the TM charge measurement the maximum dither amplitude never exceeds 1,5 V, the residual crosstalk would not be observed.

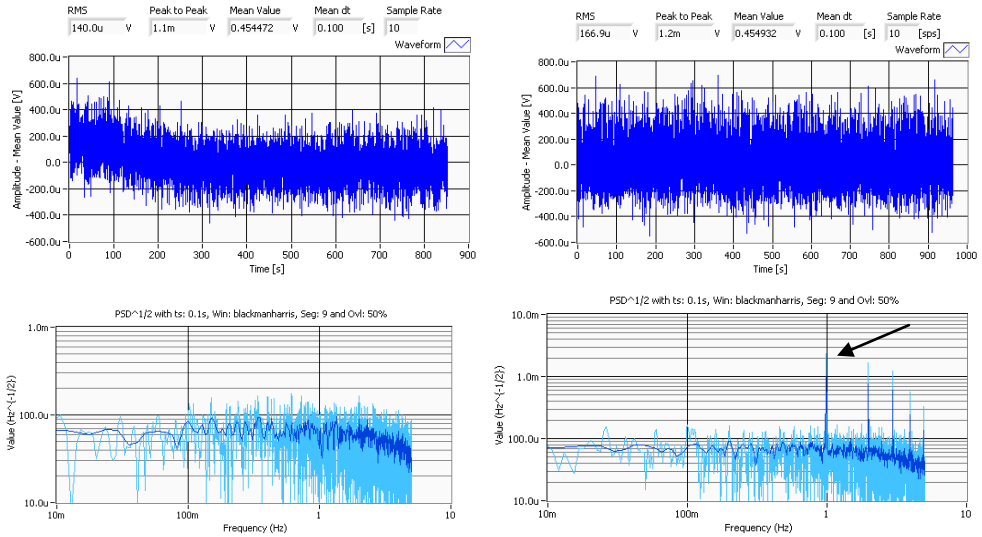

Figure 4-43 The sensing noise with 1 Hz dither at 5 V peak (left) and 50 V peak (right). The 33 times reduced dither (at 1,5 V peak) would be at the level of the white noise ($75\,\mu V/\sqrt{Hz}$)

In the second BB the board layout was modified to improve isolation of actuation and sensing circuits and isolation between sensing sub-circuits (Figure 4-3). Since the actuation passive low pass filter consists of several first order sections (three in the second BB) and the last capacitor (C_A) is part of the sensing ground, the way in which the actuation and the sensing ground are separated is crucial. The implemented layout sketch is shown in Figure 4-44.

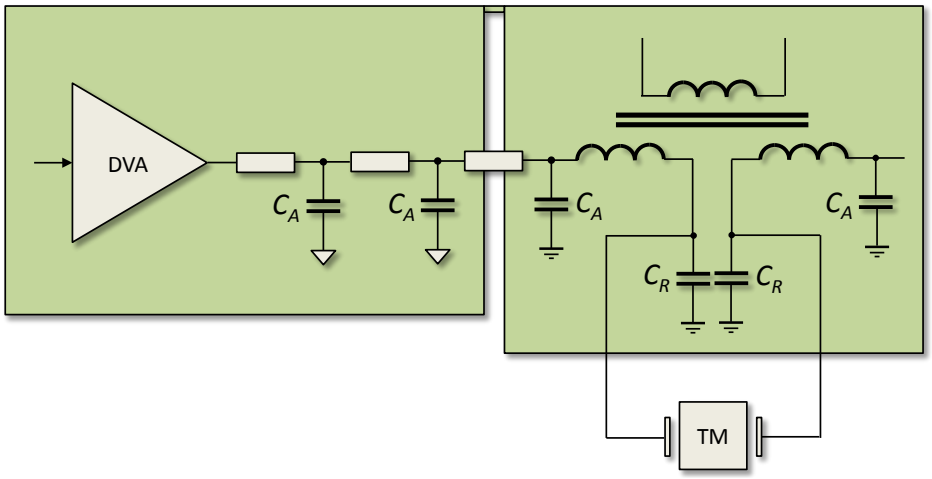

Figure 4-44 The sketch of the board grounding layout with separated actuation and sensing ground planes at the sensing bridge and connected together near the power supply. The last actuation capacitor must be as close as possible to the transformer

The crosstalk was not observed on the second breadboard. The theoretical analysis of the possible cause of the crosstalk [71] and the related debugging campaign pointed to the problem of the quality of implemented actuation capacitors (C_A in Figure 4-44). According to (2.57), the sensing offset can change if the C_A capacitor value changes and this can occur under applied voltage on the capacitor. Since large voltages of more than 100 V are applied on these capacitors, they must have at least of a 250 V rating (100 % margin for space parts).

It is also important to note that since the actuation capacitors are the low resistance path for the sensing return currents to the ground, the quality factor and their stability must be high to ensure a good overall quality factor of the bridge and its low frequency noise. It is not easy to find suitable capacitors with a high voltage rating, a high value and low losses. One can use either ceramic NPO grade capacitors or film capacitors with a good dielectric. Unfortunately, the large voltage rating NPO ceramic capacitors at 10 nF value, required for the filter circuit, are also physically large and prone to failure more easily than small ones (vibrations, board bending, etc.). In the film SMD capacitors (used on the first and second BB) the dielectric can easily separate from the electrode with repeated soldering / unsoldering and could thus also show unpredictable performance in the sensing bridge if failures are not detected.

It is known that other types of ceramic capacitors, e.g., X7R and X5R, reduce their capacitance with the applied voltage and will thus generate crosstalk in the sensing circuit. The crosstalk will appear for both step-like AC and DC or dither type actuation [71]. The examples of the crosstalk with X7R and X5R capacitors (intentionally installed) are shown in Figure 4-45.

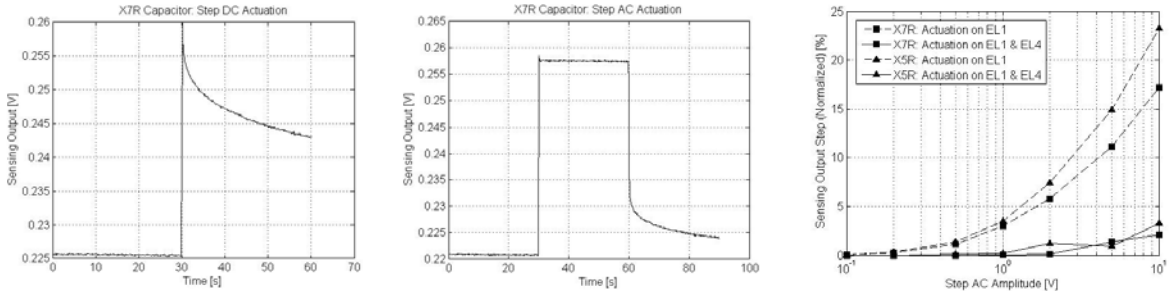

Figure 4-45 The crosstalk as a result of the 5 V DC (left plot) and 5 V peak AC (middle plot) actuation with X7R actuation capacitors. The ≈30 mV output steps are equivalent to1,2 µm (720 aF) offset shift or 12% of the nominal output, of 10 µm. The right plot shows the non-linear crosstalk when actuation is applied on single electrode (dashed lines) and not perfect cancelation when applied on both electrodes simultaneously (solid lines) for both X7R and X5R capacitors

To evaluate the crosstalk amplitude due to the dither, the amplitude spectra have been generated from the noise ASD and are shown in Figure 4-46 for the X7R ceramic and Polypropylene film capacitors.

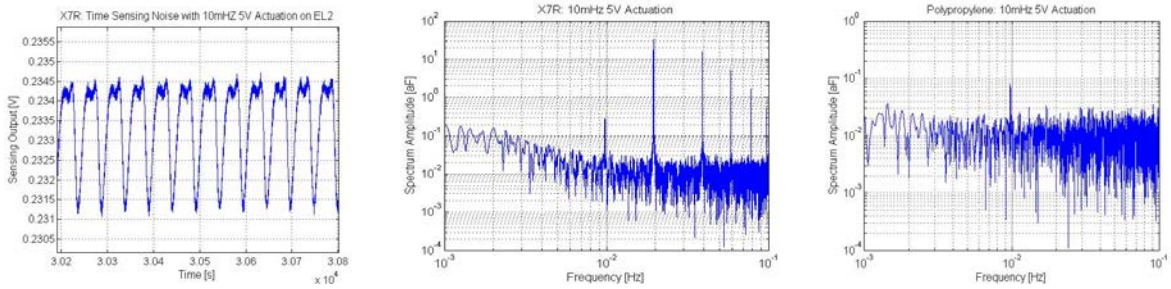

Figure 4-46 The sensing transients as a result of a 5 V peak dither at 10 mHz with X7R actuation capacitors (left plot) and the corresponding second harmonic crosstalk of 33 aF (1,4 mV) in amplitude spectrum (middle plot). The Polypropylene film capacitors produce a negligible crosstalk of 0,07 aF (right plot) at the same dither level

The crosstalk investigation showed the importance of selecting capacitors for the sensitive bridge circuit and of a careful design of the board layout, i.e., the selection of its grounding scheme.

Chapter 5
CONCLUSION

An investigation has been discussed in this dissertation aiming to set the foundation for the development of the Inertial Sensor Front End Electronics (IS-FEE) used for the sensing and control of the reference Test Mass (TM) in the spaceborne gravitational detector. This work is part of a wide scientific collaboration involving universities, institutions and industries in Europe and the United States, and constitutes a relevant part of the flight hardware development for qualifying the performances of the current LISA Pathfinder and future LISA missions.

The main design aspects are here first summarized and set in relation with the top-level scientific requirements for extremely small levels of stray acceleration needed for space-based observations of gravitational waves. Then the main scientific results in this work, based on the achieved performance of manufactured breadboards, are recalled and put in perspective for the flight hardware development by the industry.

5.1 Design Aspects

The TM position sensing in nanometer resolution and absolute accuracy of one micrometer is achieved by the IS-FEE capacitance sensing circuit in attofarad resolution. This information is then used for the spacecraft control, ensuring that the free-falling TM inside the spacecraft is always in its performance range of several micrometers around its nominal central position between sensing / actuation electrodes. The very low capacitance measurement noise of $1\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ combined with the $0{,}3\,\mathrm{fms}^{-2}/\sqrt{\mathrm{Hz}}$ sensing back-action acceleration on the TM are very stringent requirements, especially at the lowest frequency of detection, i.e., at 1 mHz for LISA Pathfinder and 0,1 mHz for LISA.

While the back-action acceleration is limited by the size of the core sensor and the proper selection of the sensing excitation voltage, the capacitance noise is fully dominated by the thermal noise due to the losses of the sensing bridge and, in particular, the differential transformer. In this work a development of the transformer with a very high quality factor (Q > 200) is discussed; all losses are investigated and analyzed both for the core selection and the coil design. No less challenging is the front-end amplifier design where different options are presented and noise sources identified.

While the TM is left free-falling in the main drag-free measurement axis, the IS-FEE is controlling the TM on other axes by applying actuation voltages on the electrodes surrounding the TM, thus generating electrostatically necessary forces and torques. The stability of actuation voltage and its DC noise, to mention the most important actuation noise sources, also introduce stray accelerations on the TM, which must be kept below $5\,\mathrm{fms}^{-2}/\sqrt{\mathrm{Hz}}$. Converted into electrical units, this is equivalent to the output voltage stability of $2\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$, which is the greatest challenge in the electronics design at a very low frequency.

The investigation in this field was concerned with the selection of the voltage reference, this being the main source of fluctuation, the digital-to-analog converter and other circuit parts ensuring low $1/f$ noise and sensitivity to temperature fluctuation. The drive voltage amplifier and the digital controller options and related trade-offs were discussed and detailed designs analyzed.

5.2 Scientific Results

The relevant sensing and actuation circuits were verified on two multi-axis breadboards manufactured in 2005 and 2010 for the torsion pendulum control at two universities in Italy. The achieved scientific results for the sensing and actuation functions are summarized in the following text.

5.2.1 Sensing Performance

The first sensing circuit was successfully built with the required performance level, although with larger noise than expected from the theoretical investigation. A thorough investigation of the noise in the sensing bridge found the excess noise in the current noise of the front-end trans-impedance amplifier. The selection of this, apparently not adequate, part for the circuit was due to an ambiguous current noise definition in the data sheet of the selected op-amp. By means of a breadboard upgrade, using the discrete JFET stage, the design was corrected and the sensing theoretical performance was achieved with noise twice below the limit.

The sensing transformer was successfully developed with a quality factor of Q = 400, i.e., again with a factor twice larger than required. Various winding techniques were investigated and the best solution suggested in relation to the very stringent 1 μm sensing offset requirement and the design which must have low stray capacitances needed to achieve a large quality factor.

For the sensing circuit verification in laboratory down to 1 mHz, the TM simulator was developed and several versions built allowing very stable differential capacitance simulation of few femtofarads.

5.2.2 Actuation Performance

Two actuation waveform options were investigated with pulsed and sinusoidal signals for which two versions of the control board electronics were successfully built and tested. Several technical notes were written in addition to this dissertation dealing with the trade-off analyses in the selection of the final actuation scheme.

To achieve very stringent noise levels at low frequencies, auto-zero amplifiers were implemented in the drive voltage amplifier circuit. Two types of the digital controllers and the low-frequency noise cancellation techniques of the digital-to-analog (DAC) and analog-to-digital converters (ADC) were studied and solutions suggested. Finally, only the analog circuits were built and verified by testing. It is important to note that the voltage reference circuit, an important contributor to the actuation stability performance, was not realized in hardware. Instead, an external instrument was used to set the voltages. Nevertheless, the performance of the amplifiers was successfully verified, as explained below.

The actuation circuits were built to achieve the LISA Pathfinder requirements at 1 mHz, but the measurements were made long enough (several days) to estimate the performance at the LISA 0,1 mHz frequency, with a view of providing a reference for future developments. The actuation DC noise level of the whole circuit was achieved by a large margin of five times and three times at 1 mHz and 0,1 mHz, respectively. With a non-zero voltage input, the noise was still at 80% of the limit at 1 mHz, but twice above the limit at 0,1 mHz, in fact due to the poor performance of the external instrument.

The actuation output instability of the amplifiers was more than three times below the limit at 1 mHz, right at the limit at 0,2 mHz and four times above the limit at 0,1 mHz. This was measured differentially to reject the fluctuation of the external instrument. During the absolute measurements the performance was also achieved with a safe margin of two at 1

mHz, but with 10 times incompliance at 0,1 mHz due to the instability of the external instrument. The next chapter will address these issues in more detail.

An important issue in the IS-FEE development is the crosstalk from the actuation to sensing circuits, which was investigated at great lengths by modeling circuits and by measurements. While the saturation of the sensing circuits at large actuation levels could be solved by tweaking the circuit's gain and filtering, the elimination of the crosstalk at attofarad level required more work in finding the source and implementing corrective actions. In the second breadboard, this was successfully achieved by the careful board layout and selection of the stable actuation filter capacitors in the sensing bridge. The crosstalk was greatly reduced to the level of 0,07 attofarad at maximum actuation voltage, which is ten times below the required limit.

5.2.3 Readiness to Proceed

The theoretical analysis and modeling of the IS-FEE circuits, including design variants were provided and the chosen designs suggested and detailed. The performance needed for the LISA Pathfinder was achieved on the breadboards. Nevertheless, more work has to be done to achieve the LISA performance at 0,1 mHz.

The know-how gained during the initial development of the electronics, summarized by this dissertation, provided enough information and confidence to proceed with the IS-FEE flight hardware development.

Chapter 6
FUTURE WORK

The LISA Pathfinder (LPF) is the technology verification mission and does not have the ambition or the means, due to its short arm length of 37 cm, to observe the gravitational waves. The electronics concerned by this dissertation was thus named the Inertial Sensor electronics. Due to the close vicinity of two TMs, the requirements were set for the performance at a ten times higher stray differential acceleration noise and in a limited frequency band down to 1 mHz. In LISA, with 5 million kilometers arm length, the detection of gravitational waves by sensing space-time fluctuation at the level of $< 10^{-21}$ is a real possibility. The sensor of the detector is therefore called the Gravity Reference Sensor (GRS) and the concerned electronics the GRS-FEE.

While the level of development and breadboarding was sufficient to enter the LPF flight hardware development, the challenges in LISA require more work. In particular, the voltage reference performance, the temperature stability of electronics, the stability of the simulators and the development of new measurement techniques to overcome the limitations in instrumentation are the most important challenges.

The most stringent requirement for LISA is the actuation stability requirement of $2\,\mathrm{ppm}/\sqrt{\mathrm{Hz}}$ at 0,1 mHz, which is dominated by the stability of the voltage reference, i.e., its $1/f$ noise. The space-qualified part discussed in the dissertation is already violating this limit by a factor of two at 0,1 mHz. The commercial parts with the required stability exist, but must be tested on radiation to prove their suitability for space. In addition, to provide some margin, at least four references must be paralleled to improve the performance by a factor of two.

The temperature stability of the reference and the electronics in general must also be improved below the 1 ppm/K level to reduce the low-frequency output noise due to the temperature fluctuation. The thermal effects can easily mask the true electronics performance during long testing needed for the verification at 0,1 mHz. The laboratory thermal environment is at least ten times more unstable than on the spacecraft. This requires further investigation of the measurement techniques, development of special test equipment and building the thermal control and test chambers for the verification of electronics.

In the sensing circuits of the GRS-FEE, the stability of parameters in the transformer bridge and the 100 kHz excitation voltage amplitude stability are the most important factors influencing performance at low frequency. A new TM simulator must be developed using more stable capacitors, e.g., based on dielectric such as air, ultra-low expansion (ULE) glass or ceramic custom designed capacitors instead of ceramic off-the-shelf capacitors. In addition, the dielectric must have very small losses so as not to reduce the quality factor of the sensing bridge. The whole simulator structure must be manufactured in stable glass-ceramic material, e.g., Zerodur, ULE, Macor or similar to ensure that not only the measurement capacitors are stable, but also the stray capacitances in the simulator enclosure that could produce artificial output fluctuation.

The performance of instruments is not satisfactory at 0,1 mHz. For example, the 8 ½ digit voltmeter from Agilent with the lowest noise in the market has low-frequency noise already four times above the limit if used to verify the voltage reference performance. Therefore, the differential measurement technique and a specially built input auto-zero amplifier are needed. Similarly, the verification of the 100 kHz injection bias amplitude stability requires a very stable demodulator since the locking amplifiers are not satisfactory for absolute measurement

and differential measurements could introduce even more noise due to phase errors and clock jitter of two signals.

The LISA Pathfinder and LISA are multi-disciplinary projects requiring full understanding of all physical phenomena by which the electronics performance might be constrained. The GRS-FEE is thus facing the greatest design challenges in the field of low noise at an ultra-low frequency, not imposed on any electronics before. It will hopefully demonstrate the free fall of the TM at an unprecedented level of its residual acceleration needed to detect gravitational waves.

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APPENDIX A

Sensing Offset Model

To account for all sensing bridge parameters influencing its asymmetry, an actuation filter circuit, as shown in Figure A-1, is added to the simple sensing transformer bridge circuit previously shown in Figure 2-3.

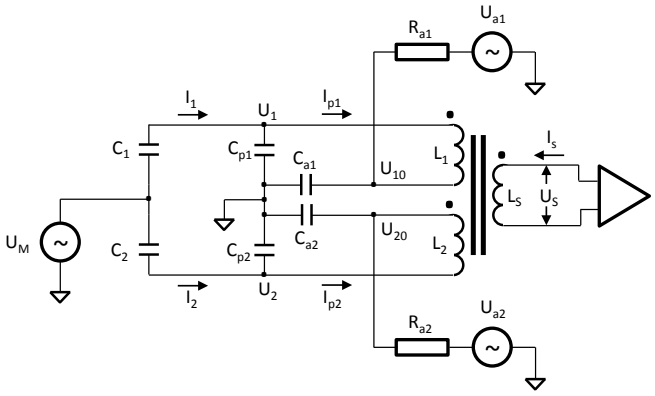

Figure A-1 Sensing bridge schematic for the purpose of sensing offset calculation

The sensing function is not significantly affected by the addition of the actuation low-pass filter consisting of resistor R_a and capacitor C_a. If this capacitance is large enough (e.g., 10 nF), then the 100 kHz sensing currents I_{p1} and I_{p2} flowing through the transformer primary windings L_1 and L_2 will still "see" in filter capacitors C_{a1} and C_{a2} a low impedance to ground. On the other hand, the actuation voltages U_{a1} and U_{a2}, being at much lower frequency or even a DC voltage, will see a high impedance in filter capacitors and will charge them to a required actuation voltage level, which will appear through the primary windings also on the terminals of C_1 and C_2, i.e., on TM electrodes.

In the offset analysis it is assumed that the actuation voltages are zero, $U_{a1} = U_{a2} = 0$, which means that the I_{p1} and I_{p2} currents will flow to the ground through the impedance Z_{a1} and Z_{a2}, defined as

$$Z_{a1} = \frac{R_{a1}}{R_{a1}C_{a1}s + 1}$$
$$Z_{a2} = \frac{R_{a2}}{R_{a2}C_{a2}s + 1} \quad \text{(A-1)}$$

Much like as in 2.1.1.1, the currents through the primary windings of the transformer can be written as

$$I_{p1} = \frac{sC_1\,U_M - s(C_1 + C_{p1})U_S}{1 + s(C_1 + C_{p1})Z_{a1}} = s\left[C_1\,U_M - (C_1 + C_{p1})U_S\right]H_1(s)$$
$$I_{p2} = \frac{sC_2\,U_M + s(C_2 + C_{p2})U_S}{1 + s(C_2 + C_{p2})Z_{a2}} = s\left[C_2\,U_M + (C_2 + C_{p2})U_S\right]H_2(s) \quad \text{(A-2)}$$

where H_1(s) and H_2(s) can be written by (A-1) as

$$H_1(\mathrm{s}) = \frac{R_{a1}C_{a1}s + 1}{R_{a1}\left(C_1 + C_{p1} + C_{a1}\right)s + 1}$$
$$H_2(\mathrm{s}) = \frac{R_{a2}C_{a2}s + 1}{R_{a2}\left(C_2 + C_{p2} + C_{a2}\right)s + 1} \tag{A-3}$$

To account for transformer inductance asymmetry, the transformer inductances and mutual inductances are defined as follows:

$$M_{1S} = K_1\sqrt{L_1L_S}\,,\ M_{2S} = K_2\sqrt{L_2L_S}$$
$$L_1 = L + \frac{\Delta L}{2},\quad L_2 = L - \frac{\Delta L}{2},\quad L_S = L \tag{A-4}$$
$$M_{1S} = K_1L\sqrt{1 + \frac{1}{2}\frac{\Delta L}{L}},\qquad M_{2S} = K_2L\sqrt{1 - \frac{1}{2}\frac{\Delta L}{L}}$$

For open transformer secondary circuit (I_S = 0), the sensing bridge output U_{BR} = U_S. By substituting (2.4) with (2.7) and (A-2), the sensing bridge voltage can be written as

$$U_{BR} = \frac{\left\{C_0[M_{1S}H_1(\mathrm{s}) - M_{2S}H_2(\mathrm{s})] + \frac{\Delta C}{2}[M_{1S}H_1(\mathrm{s}) + M_{2S}H_2(\mathrm{s})]\right\}s^2U_M}{1 + s^2\left[M_{1S}\left(C_1 + C_{p1}\right)H_1(\mathrm{s}) + M_{2S}\left(C_2 + C_{p2}\right)H_2(\mathrm{s})\right]} \tag{A-5}$$

With the following two substitutions

$$k_1 = K_1\sqrt{1 + \frac{1}{2}\frac{\Delta L}{L}},\quad k_2 = K_2\sqrt{1 - \frac{1}{2}\frac{\Delta L}{L}} \tag{A-6}$$

$$D(s) = 1 + s^2\left[M_{1S}\left(C_1 + C_{p1}\right)H_1(\mathrm{s}) + M_{2S}\left(C_2 + C_{p2}\right)H_2(\mathrm{s})\right] \tag{A-7}$$

(A-5) can be simplified to

$$U_{BR} = \left\{C_0[k_1H_1(\mathrm{s}) - k_2H_2(\mathrm{s})] + \frac{\Delta C}{2}[k_1H_1(\mathrm{s}) + k_2H_2(\mathrm{s})]\right\}\frac{s^2L}{D(s)}U_M \tag{A-8}$$

This equation can be compared with (2.6), in which the perfect symmetry of the bridge was initially modeled. The first term represents the sensing offset and the second the sensing signal proportional to the TM position, i.e., the difference in capacitance ΔC. The output of the sensing bridge will be equivalent to the sensing offset when the TM is centered with respect to electrodes, i.e., when $\Delta C = 0$.

$$U_{BR0} = C_0[k_1H_1(\mathrm{s}) - k_2H_2(\mathrm{s})]\frac{s^2L}{D(s)}U_M \tag{A-9}$$

When the offset is zero the bridge output (A-8) represents the true signal, i.e., the TM position.

$$U_{BRS} = \frac{\Delta C}{2}[k_1H_1(\mathrm{s}) + k_2H_2(\mathrm{s})]\frac{s^2L}{D(s)}U_M \tag{A-10}$$

When the TM is at the center, the input capacitances are equal: C_1 = C_2 = C_0. In addition, (A-3) can be simplified to:

$$H_1(\mathrm{s}) = \frac{R_{a1}C_{a1}s + 1}{R_{a1}\left(C_0 + C_{p1} + C_{a1}\right)s + 1} \cong \frac{C_{a1}}{C_{a1} + C_{p1}}$$
$$H_2(\mathrm{s}) = \frac{R_{a2}C_{a2}s + 1}{R_{a2}\left(C_0 + C_{p2} + C_{a2}\right)s + 1} \cong \frac{C_{a2}}{C_{a2} + C_{p2}} \tag{A-11}$$

The nominal sensing capacitance, with the TM in center position, C_0 (≈ 1 pF) is negligible compared with the bridge resonance tuning capacitor C_p (≈ 300 pF) and the actuation filter capacitor C_a (10 nF). In addition, the actuation filter resistor R_a can also be neglected because the impedance of the C_a at a resonant frequency of 100 kHz is much smaller than the parallel resistor R_a, rendering a negligible current through the R_a. With $C_p << C_a$, H_1(s) and H_2(s) have a magnitude approximately equal to one.

Substituting (A-9) with (A-6) and (A-11), one can write the condition for zero offset:

$$K_1\sqrt{1 + \frac{1}{2}\frac{\Delta L}{L}}\frac{C_{a1}}{C_{a1} + C_{p1}} = K_2\sqrt{1 - \frac{1}{2}\frac{\Delta L}{L}}\frac{C_{a2}}{C_{a2} + C_{p2}} \tag{A-12}$$

Therefore, from (A-11) and (A-12), the sources of sensing offset are the following:

- The asymmetry of transformer primary windings ($\Delta L \neq 0$)
- The asymmetry of transformer primary to secondary couplings ($K_1 \neq K_2$)
- The asymmetry of bridge resonance tuning capacitors ($C_{p1} \neq C_{p2}$)
- The asymmetry of actuation filter capacitors ($C_{a1} \neq C_{a2}$)

These parameters will set the guidelines for the differential transformer and the actuation filter design. One should note that the influence of each parameter is not the same and, therefore, their sensitivity must be further analyzed.

The offset and the output signal of the bridge, expressed by (A-9) and (A-10) as voltages, can also be expressed as input capacitance by substituting the transfer function gain $U_M\, s^2 L/D(s)$ by one.

$$C_{BR0} = C_0[k_1H_1(\mathrm{s}) - k_2H_2(\mathrm{s})]$$
$$C_{BRS} = \frac{\Delta C}{2}[k_1H_1(\mathrm{s}) + k_2H_2(\mathrm{s})] \tag{A-13}$$

To convert the input capacitance to the TM position, (A-13) must be divided by the capacitance-to-position gradient $|\partial\Delta C/\partial x|$ (2.35)

$$x_{BR0} = \frac{d}{2}[k_1H_1(\mathrm{s}) - k_2H_2(\mathrm{s})]$$
$$x_{BRS} = \frac{d}{4}\frac{\Delta C}{C_0}[k_1H_1(\mathrm{s}) + k_2H_2(\mathrm{s})] \tag{A-14}$$

First by expanding the k_1 and k_2 parameters (A-6) in Taylor series up to the first order

$$k_1 = K_1\sqrt{1 + \frac{1}{2}\frac{\Delta L}{L}} \cong K_1\left(1 + \frac{1}{4}\frac{\Delta L}{L}\right)$$
$$k_2 = K_2\sqrt{1 - \frac{1}{2}\frac{\Delta L}{L}} \cong K_2\left(1 - \frac{1}{4}\frac{\Delta L}{L}\right) \tag{A-15}$$

and then by substitution of $H_1(s)$ and $H_2(s)$ with (A-11), one can rewrite (A-14) as follows

$$\begin{aligned} x_{BR0} &\cong \frac{d}{2}\left[K_1\left(1+\frac{1}{4}\frac{\Delta L}{L}\right)\frac{C_{a1}}{C_{a1}+C_{p1}} - K_2\left(1-\frac{1}{4}\frac{\Delta L}{L}\right)\frac{C_{a2}}{C_{a2}+C_{p2}}\right] \\ x_{BRS} &\cong \frac{d}{4}\frac{\Delta C}{C_0}\left[K_1\left(1+\frac{1}{4}\frac{\Delta L}{L}\right)\frac{C_{a1}}{C_{a1}+C_{p1}} + K_2\left(1-\frac{1}{4}\frac{\Delta L}{L}\right)\frac{C_{a2}}{C_{a2}+C_{p2}}\right] \end{aligned} \tag{A-16}$$

which are the approximate models for the sensing bridge offset (x_{BR0}) and the sensing bridge signal output (x_{BRS}).

For perfectly balanced bridge parameters, i.e., $C_a = C_{a1} = C_{a2}$, $C_p = C_{p1} = C_{p2}$, $\Delta L = 0$ and $K = K_1 = K_2$ and by substituting ΔC with (2.34), the sensing bridge signal output simplifies to

$$x_{BRS} \cong x \cdot K\frac{C_a}{C_a+C_p} \tag{A-17}$$

APPENDIX B

TIA Transfer Function

The differential TIA solution is shown in Figure B-1. The TIA gain is set by the C_{FB} capacitor, where the large resistor R_{FB} is used only to prevent saturation, i.e., to construct a high-pass filter with the decoupling capacitor C_D and thus to attenuate the low frequencies.

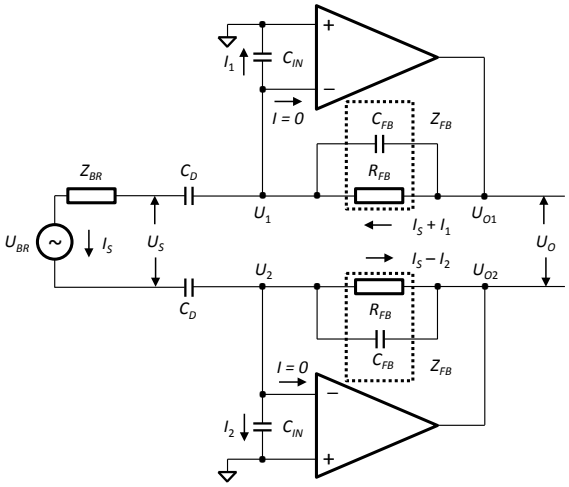

Figure B-1 Differential TIA circuit connected to the transformer secondary winding, represented by an equivalent source voltage U_{BR}, bridge impedance Z_{BR} and current I_S

It has been already seen through the simulation of the circuit (Figure 2-30) that the bandwidth of the amplifier greatly affects the transfer function. Therefore, one must depart from the ideal op-amp concept with infinite gain and include the limited op-amp open loop gain in the analysis. This means that the negative inputs of the op-amps will not be at virtual zero potential, but at U_1 and U_2, as shown in Figure B-1. In addition, the model includes the op-amp input capacitances (common and differential) and possible board stray capacitance, all represented by C_{IN}. As will be seen in APPENDIX C, this capacitance has a large influence on the resonant frequency. The currents entering op-amps are neglected because of a large internal input impedance of the FET op-amp.

Since the non-inverting TIA inputs are grounded, TIA outputs can be written as

$$U_{O1,2} = -U_{1,2}\frac{A_{OL}}{\tau s + 1} = -U_{1,2}A(s) \tag{B-1}$$

where $U_{O1,2}$ and $U_{1,2}$ are TIA output and inverting input voltages, respectively for each op-amp, A_{OL} is the DC open loop gain and τ is the time constant of the open loop gain transfer function *A(s)* that has the form of the low-pass filter. This time constant can be expressed using the op-amp bandwidth as

$$\tau = \frac{A_{OL}}{2\pi \cdot GBW} \tag{B-2}$$

Where the gain bandwidth (*GBW)* is the frequency at which the open loop gain drops to one, i.e., the standard definition of the gain bandwidth product. The inverse of the time constant is the low frequency natural corner frequency of the low-pass filter beyond which the open loop gain starts to reduce.

The equations for the currents of the upper (Figure B-1) TIA op-amp can be written as

$$I_S + I_1 = \frac{U_{O1} - U_1}{Z_{FB}}$$
$$I_1 = U_1 C_{IN} s \tag{B-3}$$

where Z_{FB} represents the impedance of the parallel combination of the feedback resistor and the capacitor. From (B-3), the voltage of the inverting TIA input can be calculated as

$$U_1 = \frac{U_{O1} - Z_{FB} I_S}{Z_{FB} C_{IN} s + 1} \tag{B-4}$$

Substituting (B-4) in (B-1), the solution for both TIA outputs is then

$$U_{O1,2} = \pm \frac{A}{1+A} \cdot \frac{Z_{FB}}{\frac{Z_{FB} C_{IN}}{1+A} s + 1} I_S \tag{B-5}$$

where $A = A(s)$ for simplicity. Consequently, the differential TIA output can be written as

$$U_O = U_{O1} - U_{O2} = \frac{A}{1+A} \cdot \frac{2Z_{FB}}{\frac{Z_{FB} C_{IN}}{1+A} s + 1} I_S \tag{B-6}$$

To calculate the secondary winding current I_S, the input circuit equation is first derived by

$$U_1 - U_2 = U_{BR} + \left(Z_{BR} + \frac{2}{C_D s} \right) I_S \tag{B-7}$$

Substituting $U_{1,2}$ with (B-1) in (B-7), the differential TIA output can be written as

$$U_O = -A \left(U_{BR} + \frac{Z_{BR} \frac{C_D}{2} s + 1}{\frac{C_D}{2} s} I_S \right) \tag{B-8}$$

Comparing (B-6) and (B-8), the solution for I_S can finally be written as

$$I_S = U_{BR} \frac{\frac{C_D}{2} s \left(\frac{Z_{FB} C_{IN}}{1+A} s + 1 \right)}{\alpha s^2 + \beta s + 1} \tag{B-9}$$

where the parameters of the denominator α and β are

$$\alpha = \frac{Z_{BR} Z_{FB} C_D C_{IN}}{2(1+A)}$$
$$\beta = \frac{2Z_{FB}(C_D + C_{IN}) + Z_{BR}(1+A) C_D}{2(1+A)} \tag{B-10}$$

Substituting I_S with (B-9) in (B-6) and dividing by U_{BR}, the TIA transfer function is

$$G_{TIA}(s) = \frac{U_O}{U_{BR}} = \frac{A}{1+A} \cdot \frac{Z_{FB} C_D s + 1}{\alpha s^2 + \beta s + 1} \tag{B-11}$$

The open loop gain factor $A/(1+A)$ is slightly less than one as A is larger than 100 (40 dB) for most of the amplifiers at 100 kHz. The nominator of the transfer function clearly shows the high-pass filter term, as expected. The TIA output is simply the TIA transfer function $G_{TIA}(s)$ multiplied by the bridge voltage U_{BR}. Note that the U_{BR} is the function of the TM injection voltage U_M and the difference in the input capacitance ΔC (2.16), and so is the TIA output.

Since α and β are functions of Z_{BR} and Z_{FB}, which are frequency dependent, the denominator of (B-11) is a very complex function. While Z_{FB} is easy to determine by

$$Z_{FB}(s) = \frac{R_{FB}}{R_{FB}C_{FB}s + 1} \tag{B-12}$$

the Z_{BR} needs more elaboration.

So far, two sensing bridge models have been developed. The first one, which was analyzed in 2.1.1, does not include the actuation capacitors C_a, but does include the real transformer winding inductance that accounts for the losses $tan\delta$ via resistance R_L. This model is described with the U_{BR} and Z_{BR} equations (2.16) and (2.17). In the second model (2.3.2 and APPENDIX A) the sensing offset was analyzed and the actuation capacitors C_a are included, but the losses in the transformer windings were not modeled to simplify analysis. To combine the models, one must refer to (A-7) and (A-8) and assume the symmetric bridge to be

$$\begin{gathered} sL_1 = sL_2 = sL_S = R_L + sL \\ M_1 = M_2 = M = K\left(\frac{R_L}{s} + L\right) \\ C_{p1} = C_{p2} = C_p \quad C_{a1} = C_{a2} = C_a \\ H_1(s) = H_2(s) = H(s) = \frac{C_a}{C_a + C_p} \end{gathered} \tag{B-13}$$

where L_1, L_2, L_S are inductances of transformer two primary and one secondary windings, respectively, M_1, M_2 and K are mutual inductances and coupling factors between the primary and secondary windings, respectively and C_{p1}, C_{p2} are the resonance tuning capacitors. With the assumptions of (B-13), (A-7) can be written as

$$D(s) = 1 + K \cdot R_L \frac{C_a C_{eq}}{C_a + C_p} s + K \cdot L \frac{C_a C_{eq}}{C_a + C_p} s^2 \tag{B-14}$$

where the equivalent capacitance C_{eq} is defined by (2.8).

Substituting (B-14) into (A-8), the bridge output voltage can be written as

$$U_{BR}(s) = K \frac{C_a}{C_a + C_p} \cdot \frac{sR_L + s^2 L}{1 + K \cdot R_L \frac{C_a C_{eq}}{C_a + C_p} s + K \cdot L \frac{C_a C_{eq}}{C_a + C_p} s^2} U_M \Delta C \tag{B-15}$$

Where coefficients k_1 and k_2 in (A-8), defined by (A-6), are equal and represented by K for the symmetric design. Similarly, by substituting (B-14) into the denominator of (2.17), the bridge impedance can be written as

$$Z_{BR}(s) = \frac{R_L + sL}{1 + K \cdot R_L \frac{C_a C_{eq}}{C_a + C_p} s + K \cdot L \frac{C_a C_{eq}}{C_a + C_p} s^2} \tag{B-16}$$

The (B-15) and (B-16) must be compared with (2.16) and (2.17) of the first model without actuation capacitors C_a. The difference is that the coefficients of the denominator have attenuating factors $K \approx 0{,}95$ and $C_a/(C_a + C_p) \approx 0{,}97$. The bridge output voltage also includes the same factors. The attenuation is logical, since any coupling between transformer primary to secondary windings less than one will attenuate the signal. Also, the 10 nF actuation capacitors C_a, located in the ground path of the primary windings are adding some resistance at 100 kHz and are reducing the common and differential primary winding currents, leading thus to a reduced secondary winding current.

Finally, by substituting (B-15) into (B-11), the TIA output can be written as

$$U_O(s) = K\frac{A}{1+A}\cdot\frac{C_\mathrm{a}}{C_\mathrm{a}+C_p}\cdot\frac{Z_{FB}C_D s+1}{\alpha s^2+\beta s+1} \cdot\frac{sR_L+s^2L}{1+K\cdot R_L\frac{C_\mathrm{a}C_{eq}}{C_\mathrm{a}+C_p}s+K\cdot L\frac{C_\mathrm{a}C_{eq}}{C_\mathrm{a}+C_p}s^2}U_M\Delta C \quad \text{(B-17)}$$

To evaluate the TIA transfer function (B-11) and its output (B-17), it is useful to substitute A with (B-1) and (B-2), Z_{BR} with (B-16) and Z_{FB} with (B-12) into α and β (B-10) and plot the functions for the bridge and TIA parameters given in Table B-1.

Table B-1 Parameters of the sensing front-end circuit using the op-amp OPA627

Parameter	Description	Value
U_M	TM peak injection voltage (100 kHz)	0,6 V
ΔC	Differential sensing capacitance for TM out off center	0,12 pF
C_0	Nominal capacitance for centered TM	1,15 pF
C_p	Tuning capacitance per bridge arm (excluding C_{IN})	324,1 pF
C_{eq}	Equivalent capacitance $2(C_0 + C_p)$	650,5 pF
C_a	Actuation capacitor per bridge arm	10 nF
L	Transformer winding inductance	4,2 mH
K	Transformer coupling between primary and secondary	0,95
Q	Transformer quality factor	200
R_L	Transformer equivalent winding resistance (related to Q)	13,2 Ω
A_{OL}	Op-amp DC open loop gain	1×10^6
BW	Op-amp bandwidth	16 MHz
u_{AMP}	Op-amp voltage noise at 10 kHz (assumed equal at 100 kHz)	$4{,}5\frac{nV}{\sqrt{Hz}}$
i_{AMP}	Op-amp current noise at 100 Hz (assumed equal at 100 kHz)[10]	$1{,}6\frac{fA}{\sqrt{Hz}}$
C_{FB}	TIA feedback capacitor	3,3 pF
R_{FB}	TIA feedback resistor	10 MΩ
C_D	TIA decoupling capacitor	20 nF
C_{IN}	TIA input capacitance	10 pF

The TIA transfer function is shown in Figure B-2.

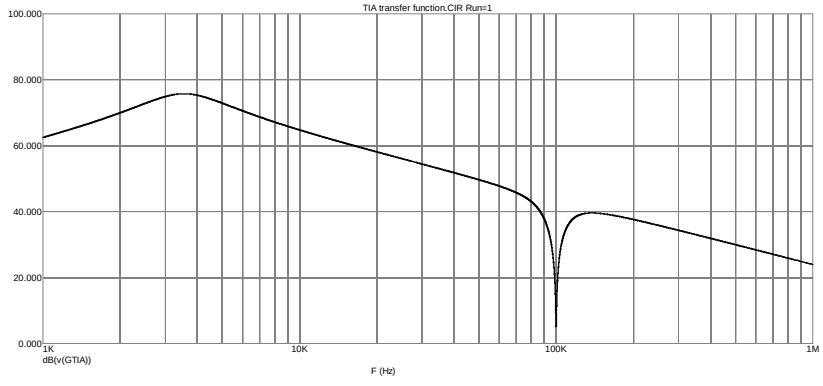

Figure B-2 The TIA transfer function $G_{TIA}(s) = U_O/U_{BR}$ (B-11) with maximum of 75,74 dB at 3,55 kHz

The zoom around 100 kHz is shown in Figure B-3.

[10] This assumption was later found to be wrong (see 4.3.1.1)

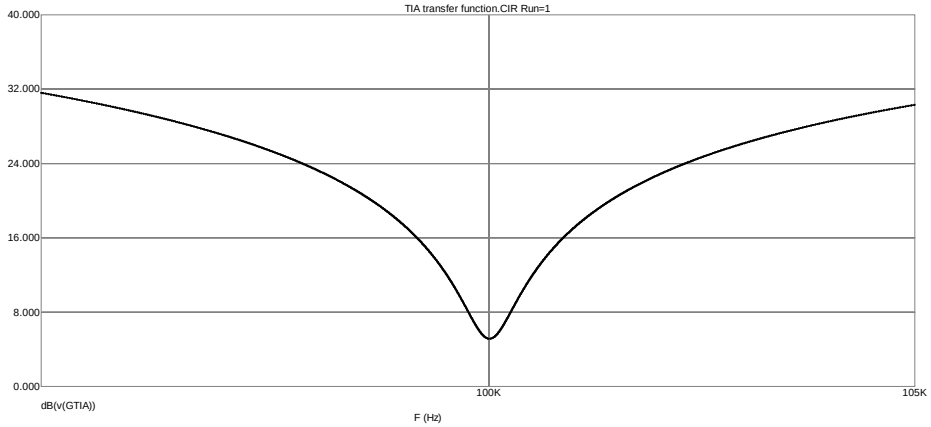

Figure B-3 Zoom of the TIA transfer function in 100 kHz ± 5 kHz range. The shape relates to the transformer quality factor Q = 200. The TIA gain at 100 kHz is 5,13 dB ≈ 1,8

The TIA output for the nominal TM injection voltage as a result of the input sensing capacitance corresponding to the full science range (0,12 pF) is shown in Figure B-4. By dividing the 39,8 mV output voltage with the input TM injection voltage of 0,6 V, the total TIA gain of 0,0663 = -23.6 dB is achieved. This result must be compared with the simulation result from Figure 2-28 (-23 dB), which confirms the mathematical model.

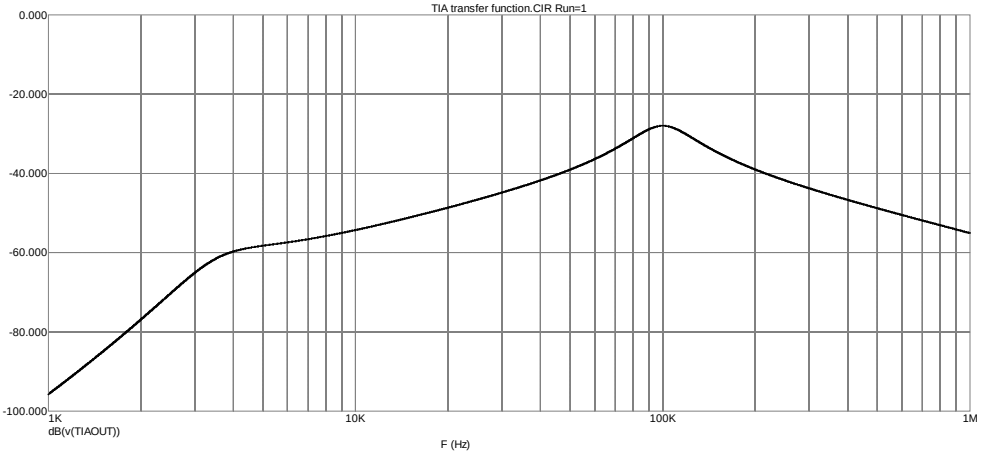

Figure B-4 The TIA output expressed in dB for the frequency range from 1 kHz to 1 MHz. The maximum amplitude at 100 kHz is -28 dB = 39,8 mV with the flatness corresponding to Q = 2,3 for the exemplary op-amp with the 16 MHz bandwidth

The accuracy of the mathematical model with respect to the op-amp bandwidth can be confirmed by comparing Figure B-5 and the simulation result from Figure 2-30. The maximum gain difference between the mathematical model and the simulation at the lowest shown frequency of 90 kHz is < 1,5 dB for all bandwidth cases.

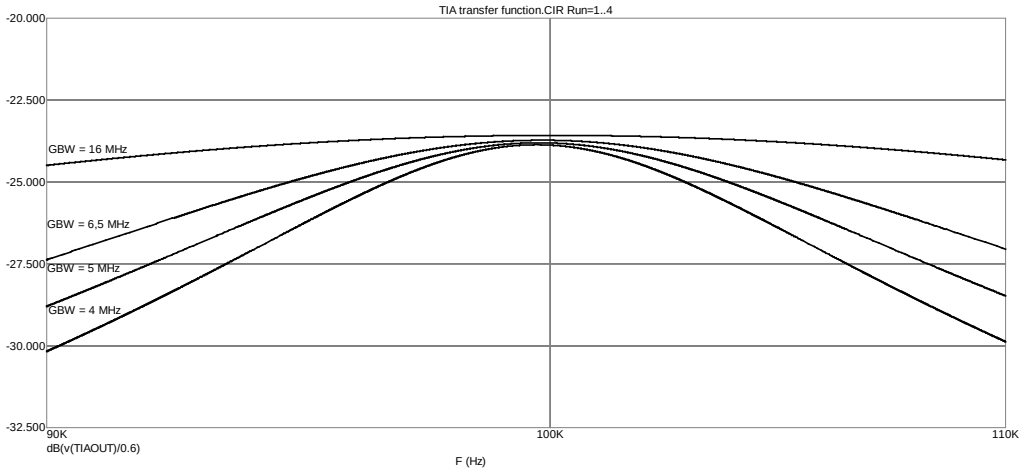

Figure B-5 The TIA output expressed in dB for the frequency range from 90 kHz to 110 kHz. The maximum amplitude at 100 kHz is -28 dB = 39,8 mV with the flatness corresponding to Q = 2,3 for the exemplary op-amp with the 16 MHz bandwidth

APPENDIX C

TIA Noise Model

C.1 Noise Sources

The TIA noise sources can be depicted from Figure C-1.

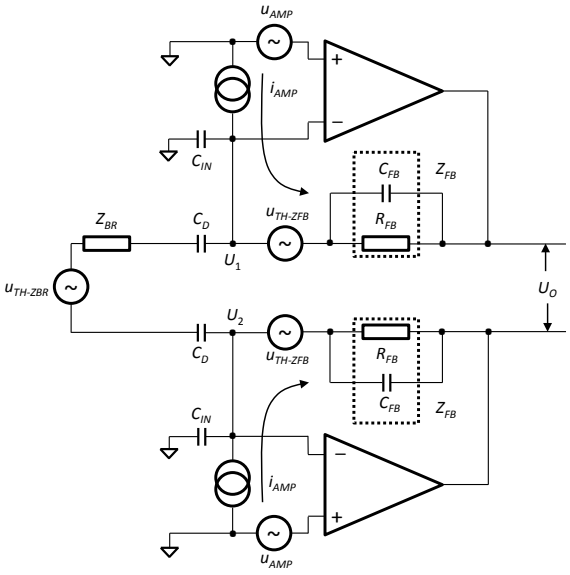

Figure C-1 The voltage, current and thermal noise sources of the TIA circuit

The total amplifier voltage noise source u_{AMP}, expressed as the voltage noise density, is shown in the non-inverting amplifier input and is transferred to the amplifier output by the amplifier noise gain that will be derived in C.2.

The amplifier current noise source i_{AMP}, expressed as the current noise density, does not generate any voltage noise in the grounded non-inverting input path of the amplifier because this path does not include any resistor. Also, this current does not flow through the input impedance (consisting of C_{IN}, C_D and Z_{BR}), as might be expected, but only through the feedback impedance Z_{FB}. The negative feedback around the amplifier works to keep the potential at the inverting amplifier input unchanged, so that a current flowing from that input is forced, by a negative feedback to flow in Z_{FB} only, resulting in a voltage $i_{AMP} \cdot Z_{FB}$. One could equally well consider the i_{AMP} flowing through the parallel combination of the input and feedback impedance and then amplify this voltage by the noise gain of the amplifier, but the result would be identical – only a more complicated calculation would be necessary.

The third group of noise sources, also expressed as the voltage noise density, is the Johnson noise or the thermal noise generated by the dissipative (real) part of the Z_{BR} and Z_{FB}, indicated by $u_{TH\text{-}ZBR}$ and $u_{TH\text{-}ZFB}$, respectively. The bridge impedance thermal noise is amplified by the TIA gain, while the feedback impedance thermal noise is directly developing at the output of the amplifier, i.e., it transfers to the output with a gain of one. The thermal noise of the complex impedance is defined by (2.24).

The uncorrelated voltage and the current and thermal noise sources of each amplifier will sum into the $\sqrt{2}$ larger differential amplifier noise. The TIA gain (B-11), which amplifies the (single) sensing bridge thermal noise, already accounts for the differential amplification factor. The output voltage noise densities can then be integrated into RMS noises in the

corresponding bandwidth and resulting individual noises added in the total TIA output; RMS noise can be written as

$$e_{TIA-RMS} = \sqrt{e_{RMS-TH}^2 + e_{RMS-u_{AMP}}^2 + e_{RMS-i_{AMP}}^2} \tag{C-1}$$

Table C-1 provides a summary of the TIA input noise sources, the conversion factors to the output and the integration bandwidth to convert the output noise density to RMS noise.

Table C-1 The TIA noise sources, the output noise density and the RMS noise conversion factors. The closed-loop bandwidth is the frequency at which the noise gain (NG) intersects the TIA open-loop gain

Input noise sources expressed as voltage noise density	Multiply by this factor to refer to differential output	Integrate in this bandwidth to convert to RMS noise
Thermal noise in Z_{BR} $\sqrt{4k_BT\Re[Z_{BR}]}$	Differential TIA gain G_{TIA}	$\frac{1}{2\pi R_{FB}C_{FB}}$
Thermal noise in Z_{FB} $\sqrt{4k_BT\Re[Z_{FB}]}$	$\sqrt{2}$	$\frac{1}{2\pi R_{FB}C_{FB}}$
Op-amp current noise on Z_{FB} $i_{AMP}\cdot\lvert Z_{FB}\rvert$	$\sqrt{2}$	$\frac{1}{2\pi R_{FB}C_{FB}}$
Op-amp voltage noise u_{AMP}	$\sqrt{2}\cdot NG$	Closed-loop bandwidth

The calculation of each noise source is provided below. Since the TIA input impedance C_{IN} is included in the TIA model, the bridge impedance (B-16) will be modified as follows

$$Z_{BR}(s) = \frac{R_L + sL}{1 + K\cdot R_L\frac{C_a C'_{eq}}{C_a + C'_p}s + K\cdot L\frac{C_a C'_{eq}}{C_a + C'_p}s^2} \tag{C-2}$$

where the tuning capacitance C'_p and the equivalent capacitance C'_e include now C_{IN}

$$C'_p = C_p + \frac{C_{IN}}{4}$$
$$C'_e = 2\left(C_0 + C_p + \frac{C_{IN}}{4}\right) \tag{C-3}$$

and where C_0 is the nominal TM capacitance with the TM centered between electrodes. The division by 4 comes from the transfer of the two input capacitances to the primary winding of the transformer, as shown in Figure C-2.

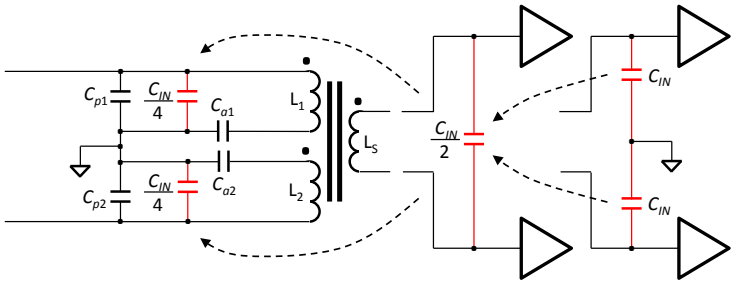

Figure C-2 The sketch of the TIA input capacitance (C_{IN} < 15 pF) and its equivalent capacitance in the transformer secondary and primary windings. The decoupling capacitors C_D are neglected due to their much larger capacitance (C_D = 20 nF)

The real part of the Z_{BR} *(s)*, used to determine the thermal noise, is plotted in Figure 2-7 and is about 528 kΩ according to Table 2-2 or the parameter values given in Table B-1. The real part of the feedback impedance, generating the thermal noise and calculated from (B-12), is

$$\Re[Z_{FB}] = \frac{R_{FB}}{1 + (\omega R_{FB} C_{FB})^2} \tag{C-4}$$

Note that this resistance (23,2 kΩ) is much smaller than the R_{FB} (10 MΩ) because the impedance of the feedback capacitance C_{FB} (3,3 pF) has considerably reduced the parallel combination $C_{FB} \parallel R_{FB}$ at 100 kHz. Therefore, the thermal noise due to the feedback resistance will be small.

The TIA current noise is flowing through the feedback impedance Z_{FB}, which is defined by

$$|Z_{FB}| = \frac{R_{FB}}{\sqrt{1 + (\omega R_{FB} C_{FB})^2}} \tag{C-5}$$

and is around 482 kΩ with parameter values of Table B-1. The op-amp current noise must thus be small so as not to generate a large output voltage noise.

The TIA voltage noise transfers to the TIA output via the noise gain, which is analyzed below.

C.2 Noise Gain

To determine the noise gain (*NG*), the signal source (U_{BR}), the op-amp current noise source (i_{AMP}) and the thermal noise ($u_{TH\text{-}ZBR}$, $u_{TH\text{-}ZFB}$) sources from Figure C-1 must be set to zero as, shown now in Figure C-3.

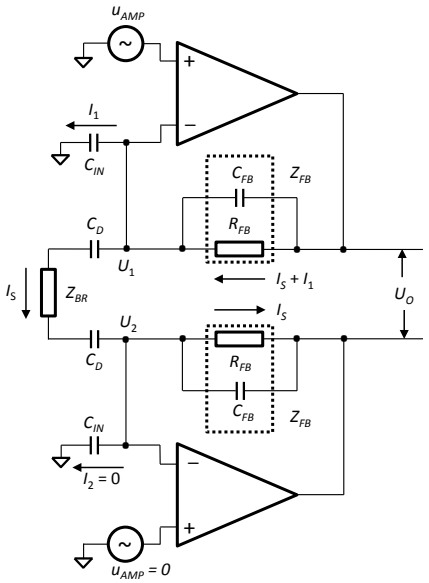

Figure C-3 The TIA voltage noise sources for the purpose of noise gain calculation of the upper amplifier

The noise gain of an op-amp is equivalent to its non-inverting signal gain, i.e.,

$$NG = 1 + \frac{Z_{FB}}{Z_{IN}} \tag{C-6}$$

where Z_{IN} is the input impedance "visible" from the inverting op-amp input.

This analysis will be simplified by the assumption that the op-amp has infinite open-loop gain and therefore identical non-inverting and inverting input voltages. Since the inverting input voltages are $U_1 = u_{AMP}$ and $U_2 = 0$, one can easily derive the circuit currents and the TIA output noise voltage due to the upper amplifier only.

$$I_1 = u_{AMP} C_{IN} s$$

$$I_S = u_{AMP} \frac{\frac{C_D}{2} s}{Z_{BR} \frac{C_D}{2} s + 1} \tag{C-7}$$

$$U_O = u_{AMP} \left[1 + \left(\frac{C_D}{Z_{BR} \frac{C_D}{2} s + 1} + C_{IN} \right) Z_{FB} s \right]$$

Therefore, the *NG* of one op-amp can be written as

$$NG = \frac{U_O}{u_{AMP}} = \frac{Z_{BR} Z_{FB} \frac{C_{IN} C_D}{2} s^2 + \left[Z_{FB}(C_{IN} + C_D) + Z_{BR} \frac{C_D}{2} \right] s + 1}{Z_{BR} \frac{C_D}{2} s + 1} \tag{C-8}$$

Note that for the large decoupling capacitor C_D and negligible input capacitance C_{IN}, the (C-8) simplifies to

$$NG_S = 1 + 2 \frac{Z_{FB}}{Z_{BR}} \tag{C-9}$$

The total voltage noise of both op-amps will thus be $NG \cdot \sqrt{2}$. It has already been stated by (2.28) that the noise PSD is further amplified by the demodulation process by factor 2 (noise ASD by factor $\sqrt{2}$). Therefore, an additional factor $\sqrt{2}$ must be included in the noise density calculation.

The plot of the *NG* (C-8) for the exemplary preamplifier and the sensing bridge with parameters defined in Table B-1 is shown in Figure C-4.

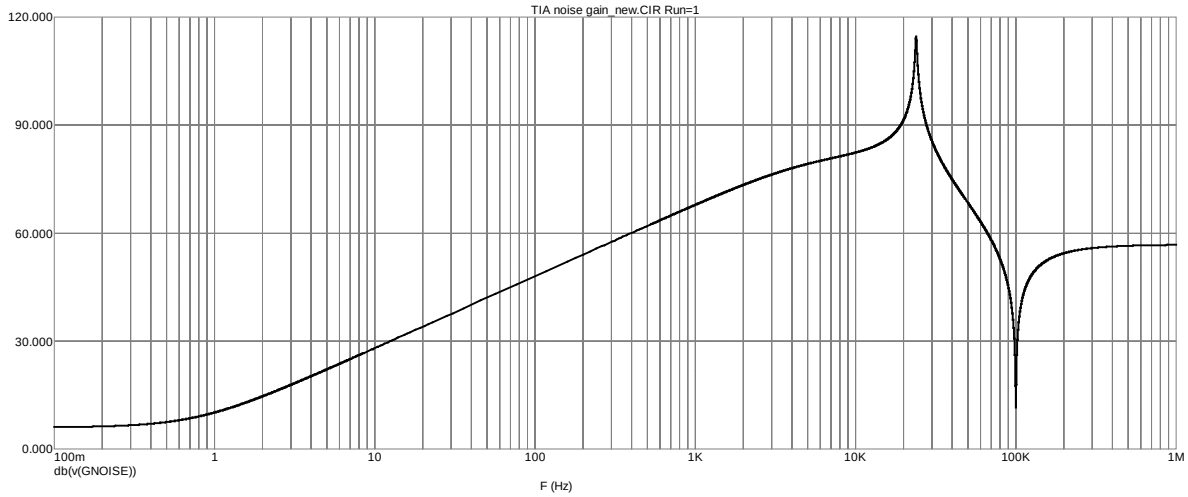

Figure C-4 The TIA noise gain in the frequency range 0,1 Hz - 1 MHz. The 11,5 dB minimum and the 114,6 dB maximum are at 100 kHz and 23,9 kHz, respectively. The DC noise gain is 6 dB, which includes the factor $\sqrt{2}$ due to the differential signaling and the factor $\sqrt{2}$ due to the demodulation process

To tune the *NG* minimum to 100 kHz, the tuning capacitance C_p (per bridge arm) has been modified from 324,1 pF (Table B-1) to 320,5 pF. The previous tuning value was used to achieve the minimum value of the TIA gain G_{TIA} and the bridge impedance Z_{BR} at 100 kHz. The C_p value does not include the op-amp input capacitance C_{IN}, but both contribute in C_p' by (C-3). The small frequency difference of two transfer function minima does not influence the principal noise analysis because the output noise is anyway tuned for its minimum.

The noise gain transfer function can be identified as follows

$$NG(s) = \frac{(T_1 s + 1)(T_4^2 s^2 + 2\xi_4 T_4 s + 1)}{(T_2 s + 1)(T_3^2 s^2 + 2\xi_3 T_3 s + 1)} \tag{C-10}$$

where the time constants of each pole and zero can be written as

$$\begin{gathered} T_1 \cong R_L C_D + R_{FB}\left(C_D + \frac{C_{FB} + C_{IN}}{2}\right) \cong R_{FB} C_D \\ T_2 = R_{FB} C_{FB} \\ T_3^2 = L\left(\frac{C_D}{2} + K\frac{C_a}{C_a + C_p'} C_{eq}'\right) \\ T_4^2 \cong L\frac{2C_D}{2C_D + C_{FB} + C_{IN}}\left(\frac{C_{FB} + C_{IN}}{2} + K\frac{C_a}{C_a + C_p'} C_{eq}'\right) \end{gathered} \tag{C-11}$$

The damping constants $\xi_{3,4}$ are very small (< 0,01), causing a very under damped response at f_3 and f_4. Note that the decoupling capacitance C_D influences mostly f_1 (0,8 Hz) and f_3 (23,9 kHz), i.e., the high-pass filter. The C_p, C_{IN} and C_{FB} influence the resonant frequency f_4 (100 kHz). The f_2 (4,8 kHz) depends only on C_{FB}. Since C_D controls at which frequency the G_{TIA} maximum appears (Figure B-4) and does not influence the frequency of the noise minimum (f_4), one can independently tune the preamplifier to achieve the lowest noise and 100 kHz and to achieve the highest and thus the most flat gain at the same frequency. The latter will reduce the temperature influence on the circuit gain.

APPENDIX D

Discrete Front-End TIA Noise Model

The noise sources of the modified TIA input stage are shown in Figure D-1. Note that the external JFET source resistance of 10 kΩ, shown in Figure 4-14, is neglected as it is paralleled by the much lower JFET drain to source resistance r_{DS}, which is 100 Ω for the selected JFET.

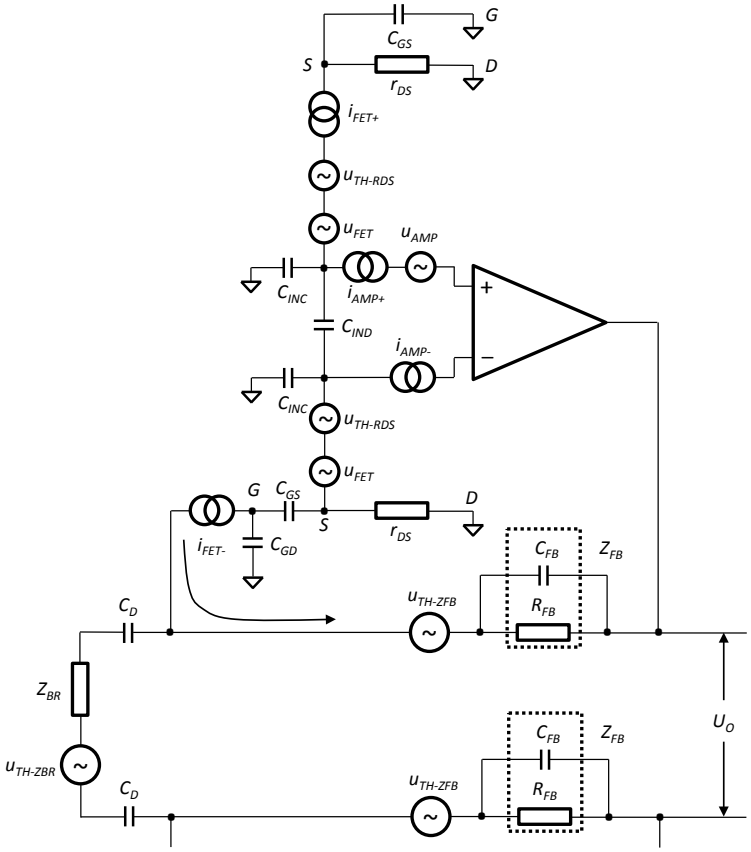

Figure D-1 The noise sources of the TIA and the discrete JFET stage. Only one half of the circuit is shown, the second being identical to the first. Labels G, D, S indicate JFET terminals gate, drain and source, respectively. Power line voltages are shorted to ground for the noise analysis

The TIA noise sources are the voltage noise u_{AMP} attributed in whole to the non-inverting input and the current noises i_{AMP+} and i_{AMP-} of the non-inverting and inverting inputs, respectively. The TIA common mode and the differential input capacitances C_{INC} and C_{IND}, respectively, are also shown. The impedance of all capacitors is much larger than that of the r_{DS} and thus the currents i_{AMP+} and i_{AMP-} are forced to flow only through r_{DS}.

The JFET noise sources are its voltage noise u_{FET}, the thermal noise due to the resistance r_{DS} u_{TH-RDS} and the current noises i_{FET+} and i_{FET-} of the JFETs attached to the non-inverting and inverting TIA inputs, respectively. The voltage and current noises consist of several contributions [66], which are described later.

The TIA feedback impedance and the transformer bridge impedance are characterized by their thermal noises u_{TH-ZFB} and u_{TH-ZBR}, respectively. The bridge impedance is real at

resonance, i.e., $Z_{BR} = R_{BR}$. Since the JFETs are configured as buffers, the noise sources can be transferred from the gate to the source with the unity gain. To simplify the analysis, all noise sources are shown in the source terminal except the i_{FET-}, which is in the gate terminal. As already explained for the initial circuit (without JFETs), this current does not flow through the input impedance (consisting of C_{GD}, C_D and Z_{BR}), as might be expected, but only through the feedback impedance Z_{FB}. The negative feedback around the amplifier works to keep the potential at the inverting amplifier input unchanged (and thus at the gate of the corresponding JFET), so that a current flowing from the gate is forced by negative feedback to flow in Z_{FB} only, resulting in a voltage $i_{FET-} \cdot Z_{FB}$.

The JFET voltage noise u_{FET} is provided in the data sheet (e_N in Table 4-5). Its low-frequency flicker noise contribution is of no interest to us since the circuit operates in AC mode due to C_D capacitors and the decoupling capacitors between the TIA and the main AC amplifier. The JFET current noise i_{FET} consists of several contributions: the i_N, which is partly correlated with voltage noise due to its transfer via the C_{GS} capacitance, the i_{SL}, the JFET gate leakage current shot noise and the i_{DIE}, the noise due to the dielectric losses of the JFET die material. All three current noise contributions for U440 JFET can be written by [66]

$$i_N = \frac{3}{8}\omega C_{GS} u_{FET} = 2{,}8\frac{fA}{\sqrt{Hz}}$$
$$i_{SL} = \sqrt{2qI_{GSS}} = 0{,}6\frac{fA}{\sqrt{Hz}} \qquad \text{(D-1)}$$
$$i_{DIE} = \sqrt{4k_B T\omega C_{DIE} tan\,\delta} = 3{,}1\frac{fA}{\sqrt{Hz}}$$

where ω is the angular frequency ($2\pi \cdot 100$ kHz), $q = 1{,}6 \times 10^{-19}$ is the electron charge, I_{GSS} = 1 pA is the gate leakage current, $k_B = 1{,}38 \times 10^{-23}$ is the Boltzmann constant, T = 300 is the temperature in Kelvin, C_{DIE} = 0,3 pF and $tan\,\delta \approx 0{,}003$ are the values for the borosilicate glass of the JFET header material [66].

The total current noise of one JFET is the RMS sum of (D-1), i.e., $i_{FET} = 4{,}2\ \mathrm{fA}/\sqrt{\mathrm{Hz}}$. A summary of parameters needed for the noise calculation is given in Table D-1.

Table D-1 JFET and TIA parameters for noise calculation

Parameter	Value	Parameter	Value
$\lvert Z_{FB}\rvert$	482 kΩ	u_{FET}	$4\ \frac{\mathrm{nV}}{\sqrt{Hz}}$
$\Re[Z_{FB}]$	23,2 kΩ	i_{FET}	$4{,}2\ \frac{\mathrm{fA}}{\sqrt{Hz}}$
R_{BR}	1,088 MΩ	u_{AMP}	$5\ \frac{\mathrm{nV}}{\sqrt{Hz}}$
r_{DS}	100 Ω	i_{AMP}	$335\ \frac{\mathrm{fA}}{\sqrt{Hz}}$

The calculation of each noise contribution for the modified TIA circuit is provided in Table D-2. The calculated values are referred to the TIA differential output and the final sensing output, for which the values at TIA output are multiplied by the sensing noise gain of 298.

Table D-2 The noise breakdown of the modified TIA circuit

Noise source	Formula	Value at TIA output	Value at sensing output
TIA voltage noise	$\sqrt{2}\cdot u_{AMP}\left(1+2\frac{\lvert Z_{FB}\rvert}{R_{BR}}\right)$	13,3 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	3,96 $\frac{\mu V}{\sqrt{Hz}}$
TIA current noise	$2\cdot i_{AMP}r_{DS}\left(1+2\frac{\lvert Z_{FB}\rvert}{R_{BR}}\right)$	0,13 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	0,04 $\frac{\mu V}{\sqrt{Hz}}$
TIA thermal noise	$\sqrt{2}\cdot\sqrt{4k_BT\Re[Z_{FB}]}$	27,7 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	8,25 $\frac{\mu V}{\sqrt{Hz}}$
JFET voltage noise	$2\cdot u_{FET}\left(1+2\frac{\lvert Z_{FB}\rvert}{R_{BR}}\right)$	15,1 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	4,50 $\frac{\mu V}{\sqrt{Hz}}$
JFET current noise	$\sqrt{2}\cdot i_{FET-}\lvert Z_{FB}\rvert$	2,9 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	0,86 $\frac{\mu V}{\sqrt{Hz}}$
JFET current noise	$\sqrt{2}\cdot i_{FET+}r_{DS}\left(1+2\frac{\lvert Z_{FB}\rvert}{R_{BR}}\right)$	0,001 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	0,00 $\frac{\mu V}{\sqrt{Hz}}$
JFET thermal noise	$2\cdot\sqrt{4k_BTr_{DS}}\left(1+2\frac{\lvert Z_{FB}\rvert}{R_{BR}}\right)$	4,9 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	1,46 $\frac{\mu V}{\sqrt{Hz}}$
Total TIA / JFET		$\mathbf{34,71\ \frac{nV}{\sqrt{Hz}}}$	$\mathbf{10,34\ \frac{\mu V}{\sqrt{Hz}}}$
Bridge thermal noise	$2\frac{\lvert Z_{FB}\rvert}{R_{BR}}\sqrt{4k_BTR_{BR}}$	118,9 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	35,43 $\frac{\mu V}{\sqrt{Hz}}$
Total noise		$\mathbf{123,86\ \frac{nV}{\sqrt{Hz}}}$	$\mathbf{36,91\ \frac{\mu V}{\sqrt{Hz}}}$

Since the noise performance was also verified in the configuration with the open TIA input, i.e., the disconnected transformer bridge, a similar calculation is provided in Table D-3. In this configuration the TIA noise gain is one.

Table D-3 The noise breakdown of the TIA circuit with the disconnected bridge

Noise source	Formula	Value at TIA output	Value at sensing output
TIA voltage noise	$\sqrt{2}\cdot u_{AMP}$	7,1 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	2,11 $\frac{\mu V}{\sqrt{Hz}}$
TIA current noise	$2\cdot i_{AMP}r_{DS}$	0,07 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	0,02 $\frac{\mu V}{\sqrt{Hz}}$
TIA thermal noise	$\sqrt{2}\cdot\sqrt{4k_BT\Re[Z_{FB}]}$	27,7 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	8,25 $\frac{\mu V}{\sqrt{Hz}}$
JFET voltage noise	$2\cdot u_{FET}$	8 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	2,38 $\frac{\mu V}{\sqrt{Hz}}$
JFET current noise	$\sqrt{2}\cdot i_{FET-}\lvert Z_{FB}\rvert$	2,9 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	0,86 $\frac{\mu V}{\sqrt{Hz}}$
JFET current noise	$\sqrt{2}\cdot i_{FET+}r_{DS}$	0,001 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	0,00 $\frac{\mu V}{\sqrt{Hz}}$
JFET thermal noise	$2\cdot\sqrt{4k_BTr_{DS}}$	2,6 $\frac{\mathrm{nV}}{\sqrt{Hz}}$	0,77 $\frac{\mu V}{\sqrt{Hz}}$
Total noise		$\mathbf{29,95\ \frac{nV}{\sqrt{Hz}}}$	$\mathbf{8,92\ \frac{\mu V}{\sqrt{Hz}}}$

ŽIVOTOPIS

Više od trideset godina iskustva na istraživanju, razvoju i konstrukciji analogne i digitalne elektronike elektro-optičkih i ultrasoničnih uređaja, inercijalnih sustava upravljanja specijalnih vozila i instrumenata za svemirska istraživanja iz područja planetologije i fundamentalne fizike

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OBRAZOVANJE I STRUČNA SPREMA

1981 – 1986	Elektrotehnički fakultet u Zagrebu, magistar znanosti iz oblasti tehničkih znanosti, područja elektrotehnike – elektronika
1973 – 1978	Fakultet elektrotehnike, stojarstva i brodogradnje u Splitu, diplomirani inženjer elektrotehnike za elektroniku

LICENCE

1999 –	P.Eng, Professional Engineers, Ontario, Canada

RADNO ISKUSTVO

2000 – *ETH Zürich, Swiss Federal Institute of Technology, Institute of Geophysics, Zürich, Switzerland*

Sistem inženjer

- Razvoj čelne elektronike inercijalnog sustava satelita za detekciju gravitacijskih valova u cilju istraživanja iz fundamentalne fizike (ESA / NASA misije: LISA Pathfinder, LISA GRS)
- Razvoj elektronike sustava za upravljanje, akviziciju i procesiranje signala različitih seizmičkih senzora za geofizička istraživanja na Marsu i Mjesecu (CNES / ESA / JAXA / NASA misije: Mars Netlander, ExoMars, Selene-2, InSight)
- Razvoj elektronike detektora i pojačala laserskog povratnog zračenja za potrebe digitalne kartografije planeta Merkura (ESA misija: Altimeter, Bepi Colombo)

1998 – 2000 *Optech Inc., Toronto, Ontario, Canada*

ALTM sistem inženjer

- Razvoj sustava za zemaljsku kartografiju iz zraka, Airborne Laser Terrestrial Mapper (ALTM)
- Konstrukcija detektora laserskog zračenja te analognih i digitalnih krugova za precizno mjerenje vremena s rezolucijom od nekoliko picosekundi
- Konstrukcija servo elektronike za 3D lasersko skaniranje

1994 – 1998 *TSI Techno Scientific Inc., Toronto, Ontario, Canada*

Vođa grupe za elektroniku

- Razvoj sustava na bazi ultrazvuka za medicinska istraživanja u ranoj detekciji mjehurića dušika u krvi ronilaca i astronauta (korišteno u misiji Space Shuttle-a)
- Razvoj elektronike ultrasoničnih sustava i instrumenata za industrijske aplikacije (mjerenje pozicije, debljine i poroznosti različitih materijala; kontrolirano raspršivanje kemikalija u agrikulturi; čišćenje sportskih pomagala)
- Konstrukcija ultrasoničnih pomagala za slijepe (stereoskopski detektor prepreka – Sonic Cane)

1992 – 1994 *Tehnički fakultet Rijeka, Hrvatska*

Asistent za predmete:

- Osnove Automatske Regulacije (elektrotehnika)
- Automatizacija i Regulacija (strojarstvo)

1979 – 1994 *FOTONA D.D. – Elekrooptika, Ljubljana, Slovenija i SOUR Rudi Čajavec – RO Profesionalna Elektronika, Banja Luka, Bosna i Hercegovina*

Glavni inženjer za sisteme

- Konstrukcija optimalnih regulatora za stabilizaciju ogledala optičkih uređaja i aktuatora različitih sustava stabilizacije
- Razvoj software-a za upravljanje i navođenje
- Razvoj i retrofit sustava za upravljanje na vozilu posebne namjene (elektro-hidraulički aktuatori, lasersko-optički daljinomjeri i inercijalni senzori za stabilizaciju sustava u pokretu)

RESUME

More than thirty years of experience in research, development and design of analog and digital electronics of electro-optical and ultrasonic equipment, control and inertial systems in special vehicles and instruments for space exploration in the fields of planetology and fundamental physics

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LICENCES

1999 –	P.Eng, Professional Engineers, Ontario, Canada

EXPERIENCE

2000 – *ETH Zürich, Swiss Federal Institute of Technology, Institute of Geophysics, Zürich, Switzerland*

System Engineer

- Development of inertial system front-end electronics for the detection of gravitational waves in the context of fundamental physics research (ESA / NASA missions: LISA Pathfinder, LISA GRS)
- Development of electronics for the control, acquisition and signal processing of various seismic sensors for geophysical exploration on Mars and the Moon (CNES / ESA / JAXA / NASA missions: Mars Netlander, ExoMars, Selene-2, InSight)
- Development of detector and amplifier electronics of the laser return pulse for the digital mapping of planet Mercury (ESA mission: Altimeter on Bepi Colombo)

1998 – 2000 *Optech Inc., Toronto, Ontario, Canada*

ALTM System Engineer

- System engineering of the Airborne Laser Terrestrial Mapper (ALTM)
- Design of a detector and a laser pulse discriminator and time interval-meter electronics with picosecond resolution
- Mirror servo electronics design of a 3D laser scanner

1994 – 1998 *TSI Techno Scientific Inc., Toronto, Ontario, Canada*

Electronics Group Leader

- Development of an ultrasonic system for medical examination and early detection of nitrogen bubbles in the blood of divers and astronauts after quick de-pressurization (used on Space Shuttle missions)
- Development of electronics of ultrasonic systems and instruments for industrial applications (measurements of position, thickness, porosity of materials, controlled spraying of chemicals in agriculture, cleaning of sporting equipment)
- Design of ultrasonic equipment to help blind people (stereoscopic detector of obstacles – Sonic Cane)

1992 – 1994 *Faculty of Engineering, University of Rijeka, Croatia*

Assistant for:

- Basics of Control Engineering (Electrical Engineering)
- Automation and Control (Mechanical Engineering)

1979 – 1994 *FOTONA D.D. – Electro-optics, Ljubljana, Slovenia and SOUR Rudi Čajavec – RO Professional Electronics, Banja Luka, Bosnia and Herzegovina*

Chief Engineer for Systems

- Optimal controller design for the stabilization of mirrors in optical equipment and design of sensors in various control systems
- Software development for control and guidance
- Development and retrofit of control systems in special vehicles (electro-hydraulic actuators, laser rangefinders, inertial sensors for moving stabilization systems)